



MS-7501 VER:3.1

CPU:

AMD M2 Athlon 64/Athlon 64 FX AM2R2

System Chipset:

AMD/ATI RS780

AMD/ATI SB700

On Board Chipset:

FINTEK Super I/O -- F71882

LAN -- RTL8111C/RTL8101E

HD Codec -- ALC888S-VC

BIOS -- SPI ROM 8M

1394 -- JMB381

Main Memory:

DDR II X 4 (Max 8GB)

Expansion Slots:

PCI-E X 16 *1

PCI-E X 1 *1

PCI 2.2 Slot X 2

Clock Generator:

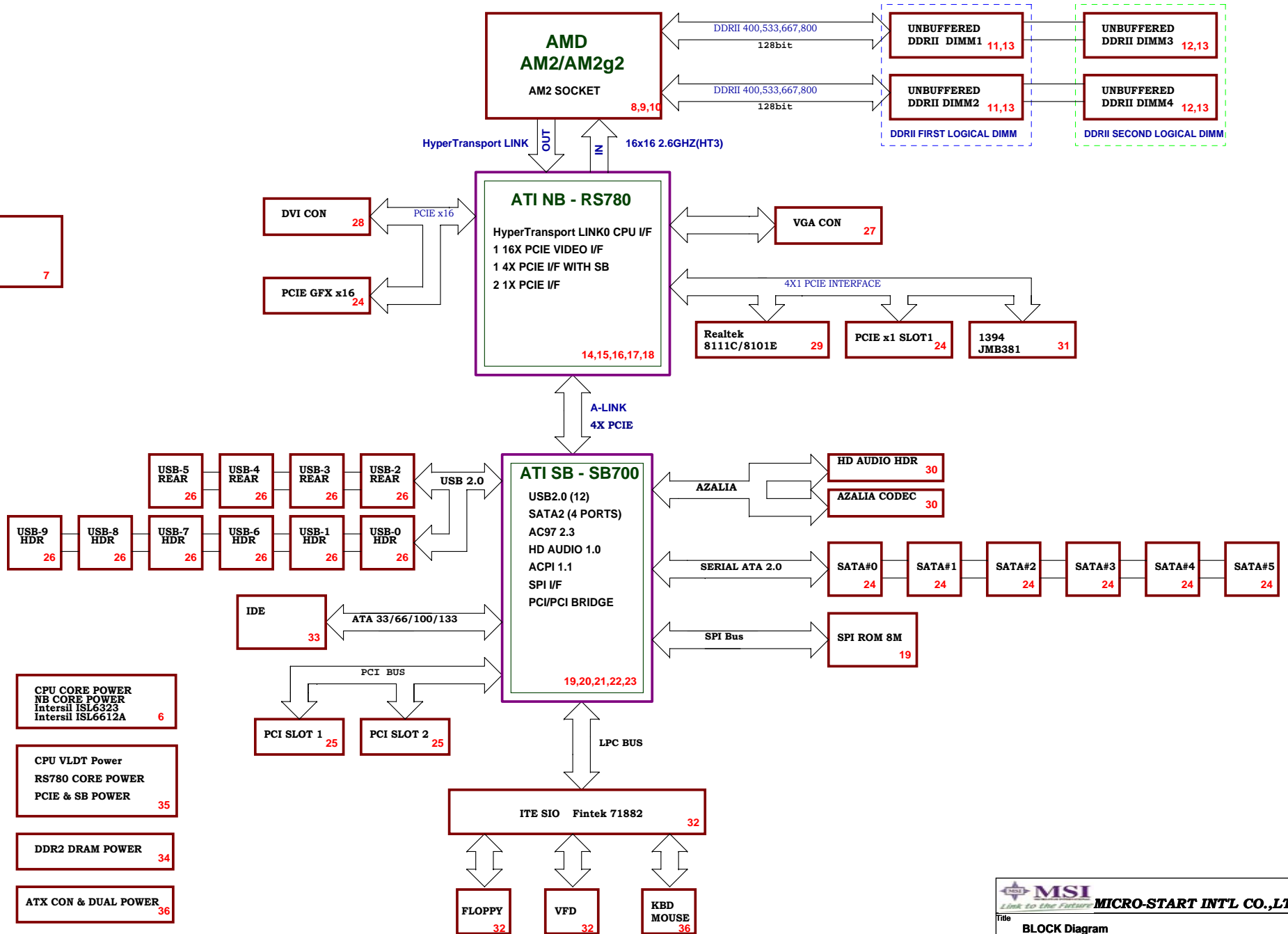
Controller--ICS9LPRS477

PWM:

Controller -- ST6740L + UP6262 4+1 Phase

Title	Page
Cover Sheet	1
Block Diagram	2
GPIO Configuration	3
Clock Distribution	4
Power Deliver Chart	5
ST6740L 4+1 Phase	6
Clock-Gen ICS9LPRS477	7
AMD AMr2 940	8, 9,10
FIRST LOGICAL DDR DIMM	11
SECOND LOGICAL DDR DIMM	12
DDR Termination	13
AMD/ATI RS780	14, 15,16,17,18
AMD/ATI SB700	19, 20,21,22,23
PCI EXPRESS X16 & X 1 SLOT	24
PCI Slot 1,2	25
USB connectors	26
VGA CONN	27
HDMI / DVI CONNECTOR	28
LAN - Realtek 8111C/8101E	29
Azalia Codec-ALC888S-VC	30
1394 Controller - JMB381	31
LPC-F71882 / FDD / VFD	32
IDE Conn / FAN	33
VCC_DDR & VCC1_1 NB	34
ACPI by UPI	35
ATX/Front Panel/KB/EMI	36
BOM - Option Parts	37
POWER OK MAP	38
RESET MAP	39
History	40

Project RS-780 BLOCK DIAGRAM



SB700 GPIO Config

GPIO Name	Type	Function Description	Pin	Page
PCICLK5/GPIO41	3.3V	PCI_CLK5	T3	17
REQ3#/GPIO70		PREQ#3	AE6	17
REQ4#/GPIO71		PREQ#4	AB6	17
GNT3#/GPIO72		Unused	AC6	17
GNT4#/GPIO73		Unused	AE5	17
INTE#/GPIO33		PCI_INTA#	AD3	17
INTF#/GPIO33		PCI_INTB#	AC4	17
INTG#/GPIO33		PCI_INTC#	AE2	17
INTH#/GPIO33		PCI_INTD#	AE3	17
LDRQ1#/GNT5#/GPIO68		Unused	AB8	17
BMREQ#/REQ5#/GPIO65		PREQ#5	AD7	17
RI#/EXTENTVNT0#		RI#	E2	18
SLP_S2/GPM9#		Unused	H7	18
GA20IN/GEVENT0#		A20GATE	Y15	18
KBRST#/GEVENT1#		KBRST#	W15	18
LPC_PME#/GEVENT3#		LPC_PME#	K4	18
LPC_SM#/#EXTENTVNT1#		LPC_SM#	K24	18
S3_STATE/GEVENT5#		Unused	F1	18
SYS_RESET#/GPM7#		FP_RST#	J2	18
WAKE#/GEVENT8#		WAKE#	H6	18
BLINK/GPM6#		Unused	F2	18
SMBALERT#/THRMTRIP#/GEVENT2#		SMBALERT#	J6	18
SATA_ISO#/GPIO10		SB_GPIO10(Strapping)	AE18	18
CLK_REQ3#/SATA_IS1#/GPIO6		SB_GPIO6(Strapping)	AD18	18
SMARTVOLT/SATA_IS2#/GPIO4		SB_GPIO4(Strapping)	AA19	18
CLK_REQ0#/SATA_IS3#/GPIO0		SB_GPIO0(Strapping)	W17	18
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39		SB_GPIO39(Strapping)	V17	18
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40		SB_GPIO40(Strapping)	W20	18
SPKR/GPIO2		SPKR	W21	18
SCL0/GPOC0#		SCLK	AA18	18
SDA0/GPOC1#		SDATA	W18	18
SCL1/GPOC2#		SCLK1	K1	18
SDA1/GPOC3#		SDATA1	K2	18
DDC1_SCL/GPIO9		Unused	AA20	18
DDC1_SDA/GPIO8		SPI_WP#	Y18	18
LLB#/GPIO66		LC_SENSE	C1	18
SHUTDOWN#/GPIO5		SB_GPIO5(Strapping)	Y19	18
DDR3_RST#/GEVENT7#		Unused	G5	18
USB_OC6#/IR_TX1/GEVENT6#		OC4#	B9	18
USB_OC5#/IR_TX0/GPM5#		OC4#	B8	18
USB_OC4#/IR_RX0/GPM4#		OC3#	A8	18
USB_OC3#/IR_RX1/GPM3#		OC3#	A9	18
USB_OC2#/GPM2#		OC2#	E5	18
USB_OC1#/GPM1#		OC2#	F8	18
USB_OC0#/GPM0#		OC1#	E4	18
AZ_SDIN0/GPIO42		SDATA_IN_R	J7	18
AZ_SDIN1/GPIO43		Unused	J8	18
AZ_SDIN2/GPIO44		Unused	L8	18
AZ_SDIN3/GPIO46		Unused	M3	18

GPIO Name	Type	Function Description	Pin	Page
AZ_DOCK_RST#/GPM8#		Unused	L5	18
PS2_DAT/EC_GPIO0		Unused	H19	18
PS2_CLK/EC_GPIO1		Unused	H20	18
SPI_CS2#/EC_GPIO2		Unused	H21	18
IDE_RST#/F_RST#/EC_GPO3		Unused	F25	18
PS2KB_DAT/EC_GPIO4		Unused	D22	18
PS2KB_CLK/EC_GPIO5		Unused	E24	18
PS2M_DAT/EC_GPIO6		Unused	E25	18
PS2M_CLK/EC_GPIO7		Unused	D23	18
USBCLK/14M_25M_48M_OSC		USB_48M_CLK	C8	18
KSO_16/EC_GPIO8		Unused	A18	18
KSO_17/EC_GPIO9		Unused	B18	18
EC_PWM0/EC_GPIO10		Unused	F21	18
SCL2/EC_GPIO11		Unused	D21	18
SDA2/EC_GPIO12		Unused	F19	18
SCL3_LV/EC_GPIO13		Unused	E20	18
SDA3_LV/EC_GPIO14		Unused	E21	18
EC_PWM1/EC_GPIO15		Unused	E19	18
EC_PWM2/EC_GPIO16		SB_GP16(Strapping)	D19	18
EC_PWM3/EC_GPIO17		Unused	E18	18
KSI_0/EC_GPIO18		Unused	G20	18
KSI_1/EC_GPIO19		Unused	G21	18
KSI_2/EC_GPIO20		Unused	D25	18
KSI_3/EC_GPIO21		Unused	D24	18
KSI_4/EC_GPIO22		Unused	C25	18
KSI_5/EC_GPIO23		Unused	C24	18
KSI_6/EC_GPIO24		Unused	B25	18
KSI_7/EC_GPIO25		Unused	C23	18
KSO_0/EC_GPIO26		Unused	B24	18
KSO_1/EC_GPIO27		Unused	B23	18
KSO_2/EC_GPIO28		Unused	A23	18
KSO_3/EC_GPIO29		Unused	C22	18
KSO_4/EC_GPIO30		Unused	A22	18
KSO_5/EC_GPIO31		Unused	B22	18
KSO_6/EC_GPIO32		Unused	B21	18
KSO_7/EC_GPIO33		Unused	A21	18
KSO_8/EC_GPIO34		Unused	D20	18
KSO_9/EC_GPIO35		Unused	C20	18
KSO_10/EC_GPIO36		Unused	A20	18
KSO_11/EC_GPIO37		Unused	B20	18
KSO_12/EC_GPIO38		Unused	B19	18
KSO_13/EC_GPIO39		Unused	A19	18
KSO_14/EC_GPIO40		Unused	D18	18
KSO_15/EC_GPIO41		Unused	C18	18
SATA_ACT#/GPIO67		SATA_LED#	W11	19
IDE_D0/GPIO15		Unused	AD24	19
IDE_D1/GPIO16		Unused	AD23	19
IDE_D2/GPIO17		Unused	AE22	19
IDE_D3/GPIO18		Unused	AC22	19

GPIO Name	Type	Function Description	Pin	Page
IDE_D4/GPIO19		Unused	AD21	19
IDE_D5/GPIO20		Unused	AE20	19
IDE_D6/GPIO21		Unused	AB20	19
IDE_D7/GPIO22		Unused	AD19	19
IDE_D8/GPIO23		Unused	AE19	19
IDE_D9/GPIO24		Unused	AC20	19
IDE_D10/GPIO25		Unused	AD20	19
IDE_D11/GPIO26		Unused	AE21	19
IDE_D12/GPIO27		Unused	AB22	19
IDE_D13/GPIO28		Unused	AD22	19
IDE_D14/GPIO29		Unused	AE23	19
IDE_D15/GPIO30		Unused	AC23	19
SPI_DI/GPIO12		SPI_DATAIN	G6	19
SPI_DO/GPIO11		SPI_DATAOUT	D2	19
SPI_CLK/GPIO47		SPI_CLK	D1	19
SPI_HOLD#/GPIO31		SPI_HOLD_L	F4	19
SPI_CS#/GPIO32		SPI_CS#	F3	19
LAN_RST#/GPIO13		CPU_PRESENT#	U15	19
ROM_RST#/GPIO14		Unused	J1	19
FANOUT0/GPIO3		Unused	M8	19
FANOUT1/GPIO48		COM_GPIO	M5	19
FANOUT2/GPIO49		Unused	M7	19
FANIN0/GPIO50		Unused	P5	19
FANIN1/GPIO51		Unused	P8	19
FANIN2/GPIO52		Unused	E8	19
TEMPIN0/GPIO61		Unused	B6	19
TEMPIN1/GPIO62		Unused	A6	19
TEMPIN2/GPIO63		Unused	A5	19
TEMPIN3/TALERT#/GPIO64		TALERT#	B5	19
VIN0/GPIO53		BIOS_WP#1	A4	19
VIN1/GPIO54		BIOS_WP#2	B4	19
VIN2/GPIO55		CLR_COMS	C4	19
VIN3/GPIO56		LAN_DISABLE	D4	19
VIN4/GPIO57		Unused	D5	19
VIN5/GPIO58		Unused	D6	19
VIN6/GPIO59		Unused	A7	19
VIN7/GPIO60		Unused	B7	19

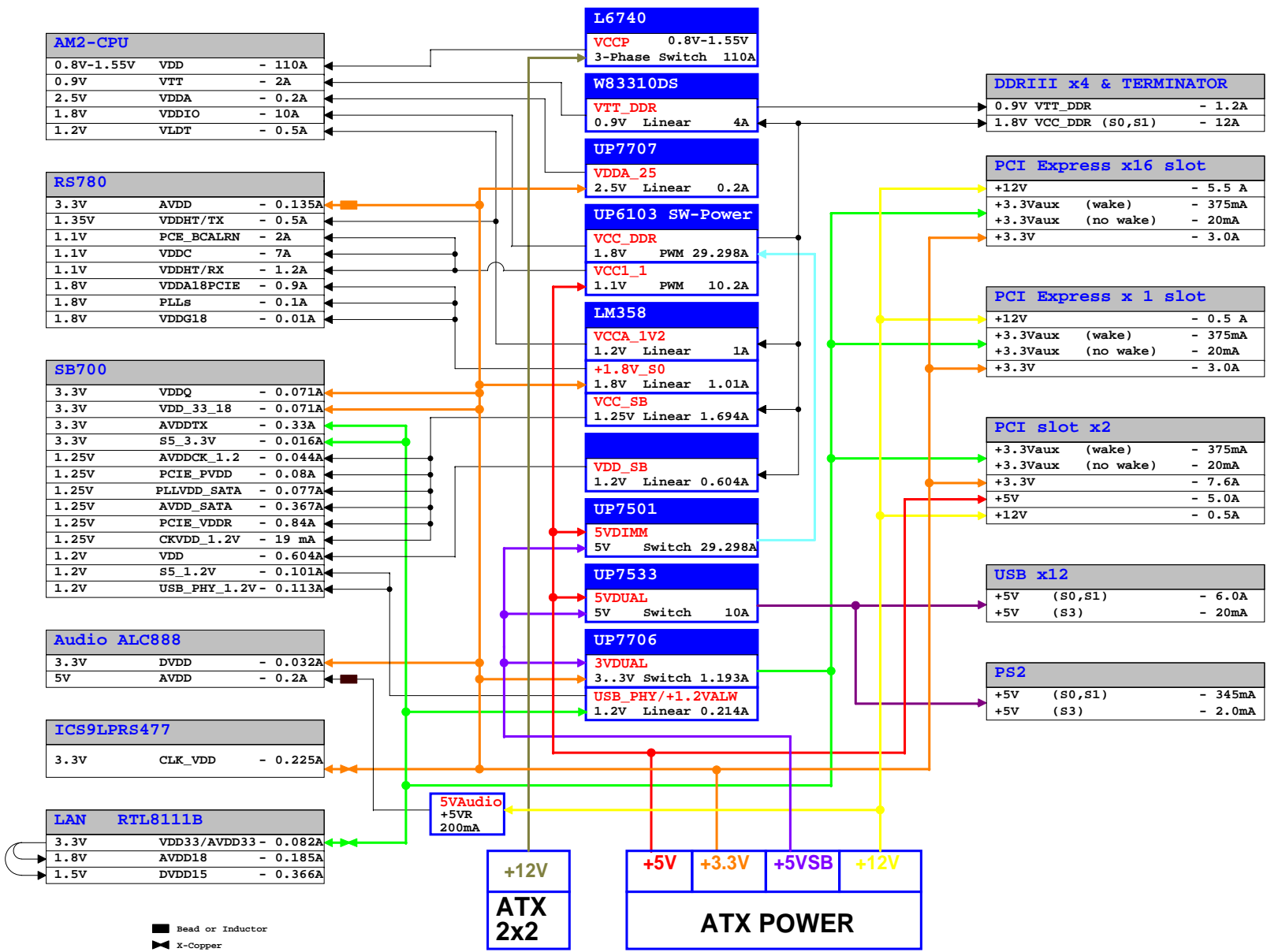
Super I/O GPIO Config

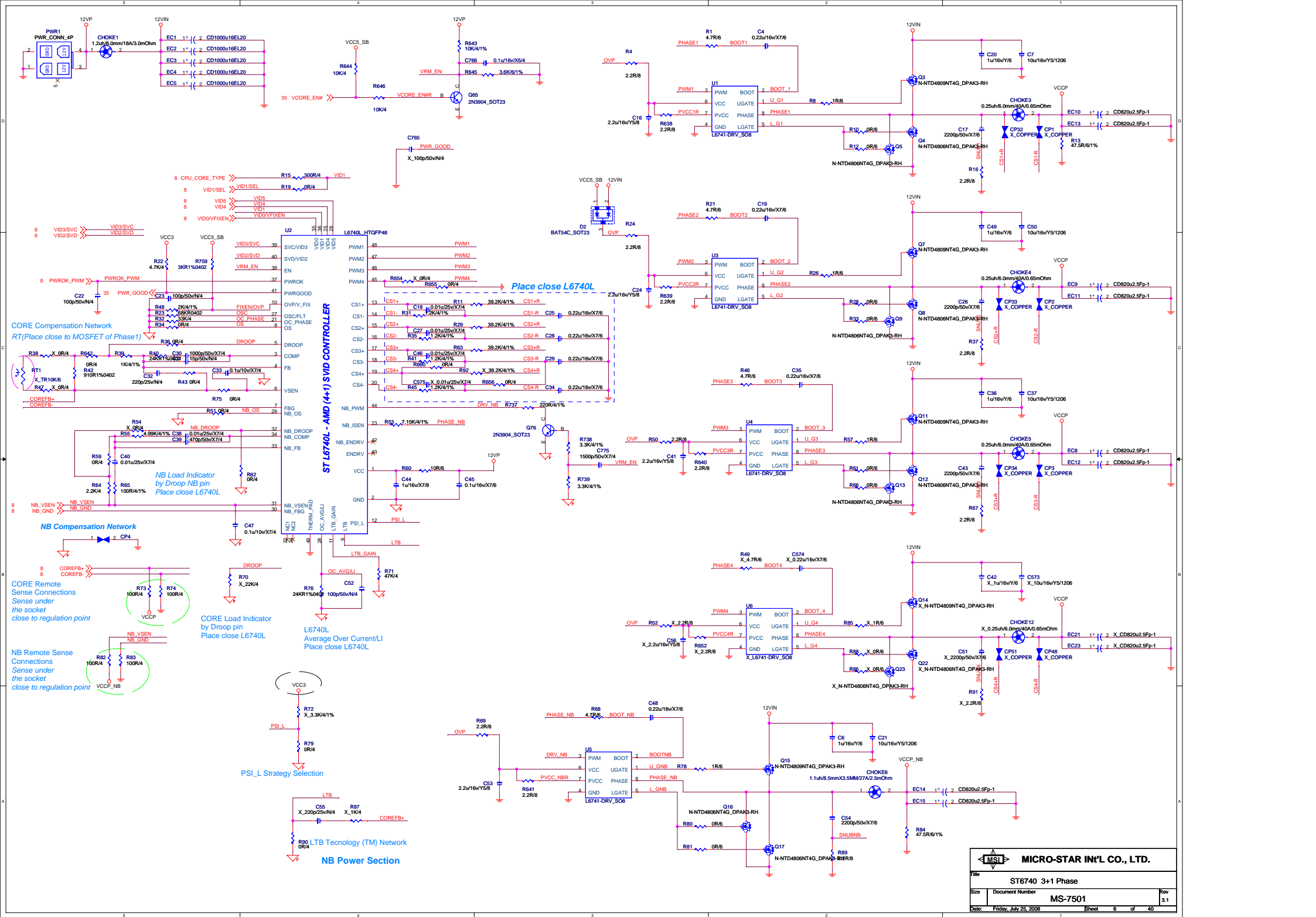
GPIO Name	Type	Function Description	Pin	Page
VID05/GP27		LEO_GPIO2	20	26
VID04/GP26		LEO_GPIO1	21	26
VID01/GP21/VGP0		LEO_GPIO0	26	26
PME#/GP54		LPC_PME#	73	26
KRST#/GP62		KBRST#	45	26
GA20/JP7		A20GATE	46	26
KDAT/GP61		KBDATA	80	26
KCLK/GP60		KBCLK	81	26
MDAT/GP57		MSDATA	82	26
MCLK/GP56		MSCLK	83	26
SUSC#/GP53		LPC_SM#	77	26
PSON#/GP42		PS_ON#	76	26
PANSWH#/GP43		PSIN	75	26
PWRON#/GP44		SB_PWRON#	72	26
PCIRST3#/GP11		ASSID_GPIO0	34	26
PCIRST2#/GP12		ASSID_GPIO1	33	26
FAN_CTL3/GP36		PWRFAN_PWM	12	26
FAN_TAC3/GP37		PWRFAN_TAC	11	26
FAN_CTL2/GP51		SYSFAN_PWM	10	26
FAN_TAC2/GP52		SYSFAN_TAC	9	26
FAN_CTL1		CPUFAN_PWM	8	26
FAN_TAC1		CPUFAN_TAC	7	26
VID2/GP32		COM_GPIO2	17	26
VID3/GP33		FUSB_G1	16	26
VID4/GP34		FUSB_G2	14	26
VID5/GP35		FUSB_G3	13	26

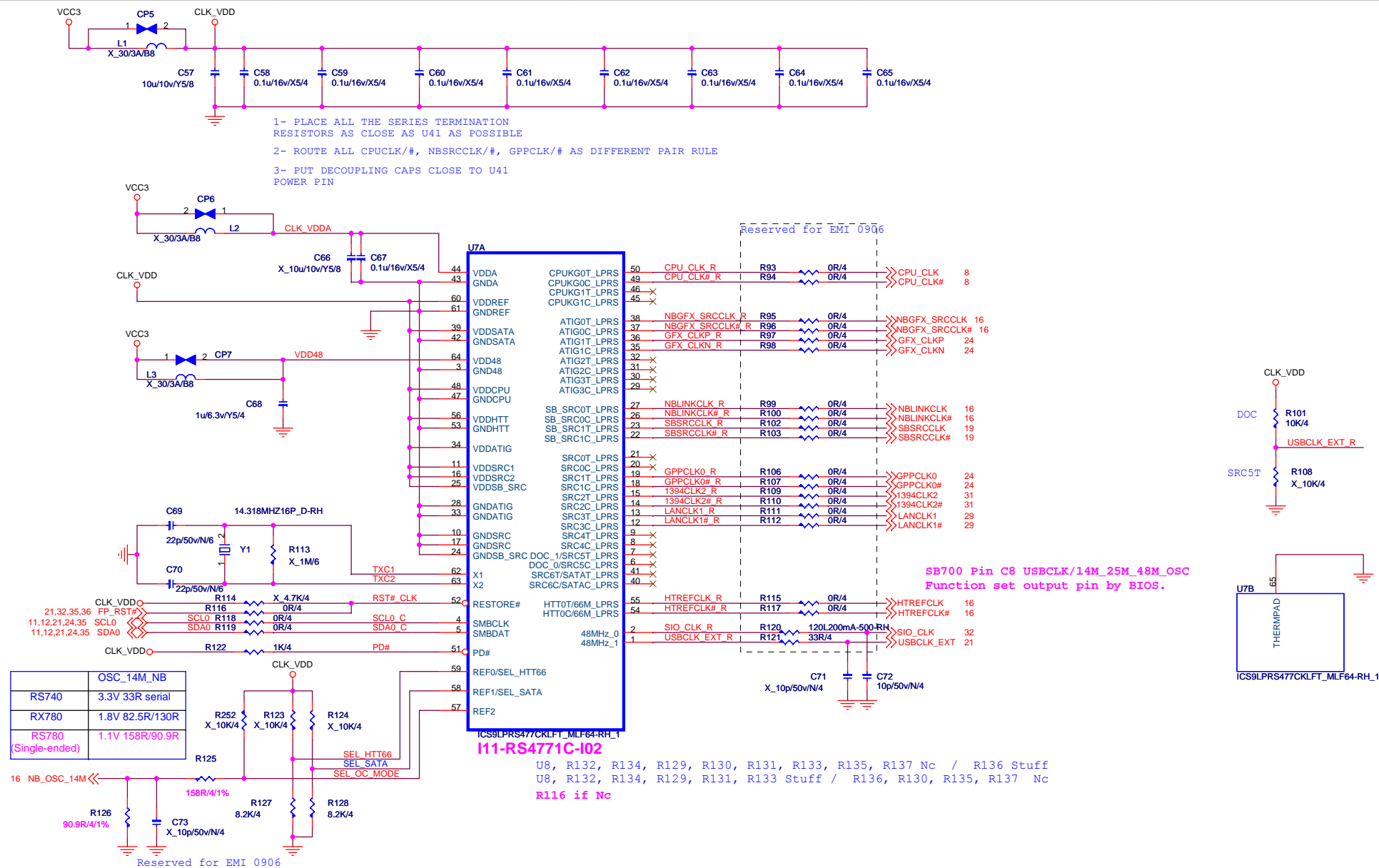
PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INTE# PCI_INTF# PCI_INTG# PCI_INTH#	PREQ#0 PGNT#0	AD18	PCICLK0
PCI Slot 2	PCI_INTF# PCI_INTG# PCI_INTH# PCI_INTE#	PREQ#1 PGNT#1	AD19	PCICLK1
PCI Slot 1	PCI_INTG# PCI_INTH# PCI_INTE# PCI_INTF#	PREQ#2 PGNT#2	AD17	PCICLK2

Power Deliver Chart

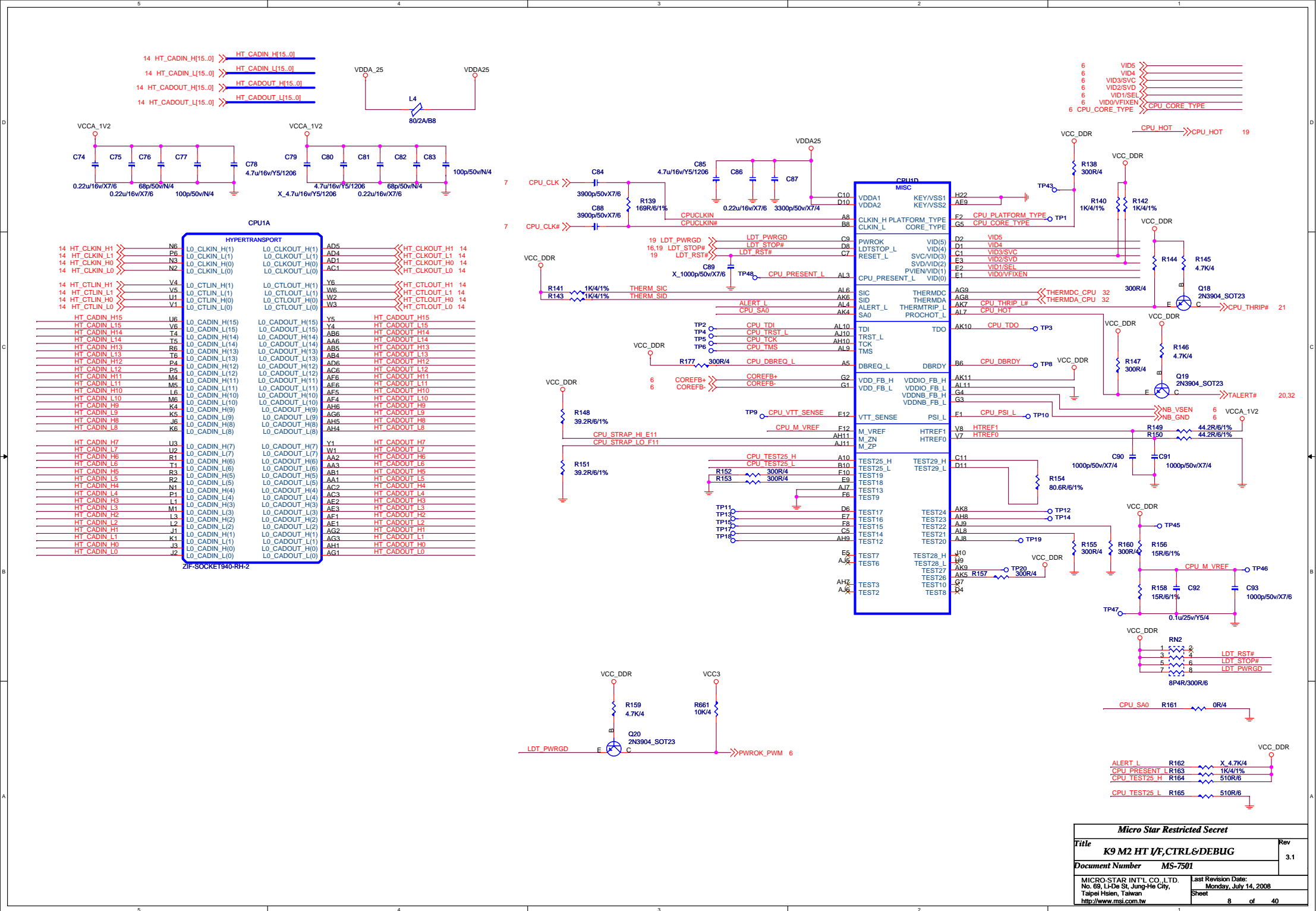






EXT CLK FREQUENCY SELECT TABLE(MHZ)	
REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal HAMMER operation



11,12 MEM_MA_DQS_L[7..0] >> MEM_MA_DQS_L[7..0]
11,12 MEM_MA_DQS_H[7..0] >> MEM_MA_DQS_H[7..0]
11,12 MEM_MA_DM[7..0] >> MEM_MA_DM[7..0]
11,12,13 MEM_MA_ADD[15..0] >> MEM_MA_ADD[15..0]
11,12 MEM_MA_DATA[63..0] >> MEM_MA_DATA[63..0]

11,12 MEM_MB_DQS_L[7..0] >> MEM_MB_DQS_L[7..0]
11,12 MEM_MB_DQS_H[7..0] >> MEM_MB_DQS_H[7..0]
11,12 MEM_MB_DM[7..0] >> MEM_MB_DM[7..0]
11,12,13 MEM_MB_ADD[15..0] >> MEM_MB_ADD[15..0]
11,12 MEM_MB_DATA[63..0] >> MEM_MB_DATA[63..0]

CPU1B

MEMORY INTERFACE A

11,13 MEM_MA0_CLK_H2	>>	MEM_MA0_CLK_H2	AG21	MA0_CLK_H(2)	MA_DATA(63)
11,13 MEM_MA0_CLK_L2	>>	MEM_MA0_CLK_L2	AG20	MA0_CLK_L(2)	MA_DATA(62)
11,13 MEM_MA0_CLK_H1	>>	MEM_MA0_CLK_H1	G19	MA0_CLK_H(1)	MA_DATA(61)
11,13 MEM_MA0_CLK_L1	>>	MEM_MA0_CLK_L1	H19	MA0_CLK_L(1)	MA_DATA(60)
11,13 MEM_MA0_CLK_H0	>>	MEM_MA0_CLK_H0	U27	MA0_CLK_H(0)	MA_DATA(59)
11,13 MEM_MA0_CLK_L0	>>	MEM_MA0_CLK_L0	U26	MA0_CLK_L(0)	MA_DATA(58)
11,13 MEM_MA0_CS_L1	>>	MEM_MA0_CS_L1	AC25	MA0_CS_L(1)	MA_DATA(57)
11,13 MEM_MA0_CS_L0	>>	MEM_MA0_CS_L0	AA24	MA0_CS_L(0)	MA_DATA(56)
11,13 MEM_MA0_ODT0	>>	MEM_MA0_ODT0	AC28	MA0_ODT(0)	MA_DATA(54)
12,13 MEM_MA1_CLK_H2	>>	MEM_MA1_CLK_H2	AE20	MA1_CLK_H(2)	MA_DATA(53)
12,13 MEM_MA1_CLK_L2	>>	MEM_MA1_CLK_L2	AE19	MA1_CLK_L(2)	MA_DATA(52)
12,13 MEM_MA1_CLK_H1	>>	MEM_MA1_CLK_H1	G20	MA1_CLK_H(1)	MA_DATA(51)
12,13 MEM_MA1_CLK_L1	>>	MEM_MA1_CLK_L1	G21	MA1_CLK_L(1)	MA_DATA(50)
12,13 MEM_MA1_CLK_H0	>>	MEM_MA1_CLK_H0	V27	MA1_CLK_H(0)	MA_DATA(49)
12,13 MEM_MA1_CLK_L0	>>	MEM_MA1_CLK_L0	W27	MA1_CLK_L(0)	MA_DATA(48)
12,13 MEM_MA1_CS_L1	>>	MEM_MA1_CS_L1	AD27	MA1_CS_L(1)	MA_DATA(47)
12,13 MEM_MA1_CS_L0	>>	MEM_MA1_CS_L0	AA25	MA1_CS_L(0)	MA_DATA(46)
12,13 MEM_MA1_ODT0	>>	MEM_MA1_ODT0	AC27	MA1_ODT(0)	MA_DATA(44)
11,12,13 MEM_MA_CAS_L	>>	MEM_MA_CAS_L	AB25	MA_CAS_L	MA_DATA(43)
11,12,13 MEM_MA_WE_L	>>	MEM_MA_WE_L	AB27	MA_WE_L	MA_DATA(42)
11,12,13 MEM_MA_RAS_L	>>	MEM_MA_RAS_L	AA26	MA_RAS_L	MA_DATA(41)
11,12,13 MEM_MA_BANK2	>>	MEM_MA_BANK2	N25	MA_BANK(2)	MA_DATA(39)
11,12,13 MEM_MA_BANK1	>>	MEM_MA_BANK1	Y27	MA_BANK(1)	MA_DATA(38)
11,12,13 MEM_MA_BANK0	>>	MEM_MA_BANK0	AA27	MA_BANK(0)	MA_DATA(37)
12,13 MEM_MA_CKE1	>>	MEM_MA_CKE1	L27	MA_CKE(1)	MA_DATA(36)
11,13 MEM_MA_CKE0	>>	MEM_MA_CKE0	M25	MA_CKE(0)	MA_DATA(35)
MEM_MA_ADD15	>>	MEM_MA_ADD15	M27	MA_ADD(15)	MA_DATA(34)
MEM_MA_ADD14	>>	MEM_MA_ADD14	N24	MA_ADD(14)	MA_DATA(33)
MEM_MA_ADD13	>>	MEM_MA_ADD13	AC26	MA_ADD(13)	MA_DATA(32)
MEM_MA_ADD12	>>	MEM_MA_ADD12	N26	MA_ADD(12)	MA_DATA(31)
MEM_MA_ADD11	>>	MEM_MA_ADD11	P25	MA_ADD(11)	MA_DATA(30)
MEM_MA_ADD10	>>	MEM_MA_ADD10	Y25	MA_ADD(10)	MA_DATA(29)
MEM_MA_ADD9	>>	MEM_MA_ADD9	N27	MA_ADD(9)	MA_DATA(28)
MEM_MA_ADD8	>>	MEM_MA_ADD8	R24	MA_ADD(8)	MA_DATA(27)
MEM_MA_ADD7	>>	MEM_MA_ADD7	P27	MA_ADD(7)	MA_DATA(26)
MEM_MA_ADD6	>>	MEM_MA_ADD6	R25	MA_ADD(6)	MA_DATA(25)
MEM_MA_ADD5	>>	MEM_MA_ADD5	R26	MA_ADD(5)	MA_DATA(24)
MEM_MA_ADD4	>>	MEM_MA_ADD4	R27	MA_ADD(4)	MA_DATA(23)
MEM_MA_ADD3	>>	MEM_MA_ADD3	T25	MA_ADD(3)	MA_DATA(22)
MEM_MA_ADD2	>>	MEM_MA_ADD2	U25	MA_ADD(2)	MA_DATA(21)
MEM_MA_ADD1	>>	MEM_MA_ADD1	T27	MA_ADD(1)	MA_DATA(20)
MEM_MA_ADD0	>>	MEM_MA_ADD0	W24	MA_ADD(0)	MA_DATA(19)
MEM_MA_DQS_H7	>>	MEM_MA_DQS_H7	AD15	MA_DQS_H(7)	MA_DATA(18)
MEM_MA_DQS_L7	>>	MEM_MA_DQS_L7	AE15	MA_DQS_L(7)	MA_DATA(17)
MEM_MA_DQS_H6	>>	MEM_MA_DQS_H6	AG18	MA_DQS_H(6)	MA_DATA(16)
MEM_MA_DQS_L6	>>	MEM_MA_DQS_L6	AG19	MA_DQS_L(6)	MA_DATA(15)
MEM_MA_DQS_H5	>>	MEM_MA_DQS_H5	AG24	MA_DQS_H(5)	MA_DATA(14)
MEM_MA_DQS_L5	>>	MEM_MA_DQS_L5	AG25	MA_DQS_L(5)	MA_DATA(13)
MEM_MA_DQS_H4	>>	MEM_MA_DQS_H4	AG27	MA_DQS_H(4)	MA_DATA(12)
MEM_MA_DQS_L4	>>	MEM_MA_DQS_L4	AG28	MA_DQS_L(4)	MA_DATA(11)
MEM_MA_DQS_H3	>>	MEM_MA_DQS_H3	D29	MA_DQS_H(3)	MA_DATA(10)
MEM_MA_DQS_L3	>>	MEM_MA_DQS_L3	C29	MA_DQS_L(3)	MA_DATA(9)
MEM_MA_DQS_H2	>>	MEM_MA_DQS_H2	D25	MA_DQS_H(2)	MA_DATA(8)
MEM_MA_DQS_L2	>>	MEM_MA_DQS_L2	C25	MA_DQS_L(2)	MA_DATA(7)
MEM_MA_DQS_H1	>>	MEM_MA_DQS_H1	E19	MA_DQS_H(1)	MA_DATA(6)
MEM_MA_DQS_L1	>>	MEM_MA_DQS_L1	F19	MA_DQS_L(1)	MA_DATA(5)
MEM_MA_DQS_H0	>>	MEM_MA_DQS_H0	F15	MA_DQS_H(0)	MA_DATA(4)
MEM_MA_DQS_L0	>>	MEM_MA_DQS_L0	G15	MA_DQS_L(0)	MA_DATA(3)
MEM_MA_DM7	>>	MEM_MA_DM7	AE15	MA_DM(7)	MA_DATA(2)
MEM_MA_DM6	>>	MEM_MA_DM6	AE19	MA_DM(6)	MA_DATA(1)
MEM_MA_DM5	>>	MEM_MA_DM5	AJ25	MA_DM(5)	MA_DATA(0)
MEM_MA_DM4	>>	MEM_MA_DM4	AH29	MA_DM(4)	MA_CHECK(7)
MEM_MA_DM3	>>	MEM_MA_DM3	B29	MA_DM(3)	MA_CHECK(6)
MEM_MA_DM2	>>	MEM_MA_DM2	E24	MA_DM(2)	MA_CHECK(5)
MEM_MA_DM1	>>	MEM_MA_DM1	E18	MA_DM(1)	MA_CHECK(4)
MEM_MA_DM0	>>	MEM_MA_DM0	H15	MA_DM(0)	MA_CHECK(3)

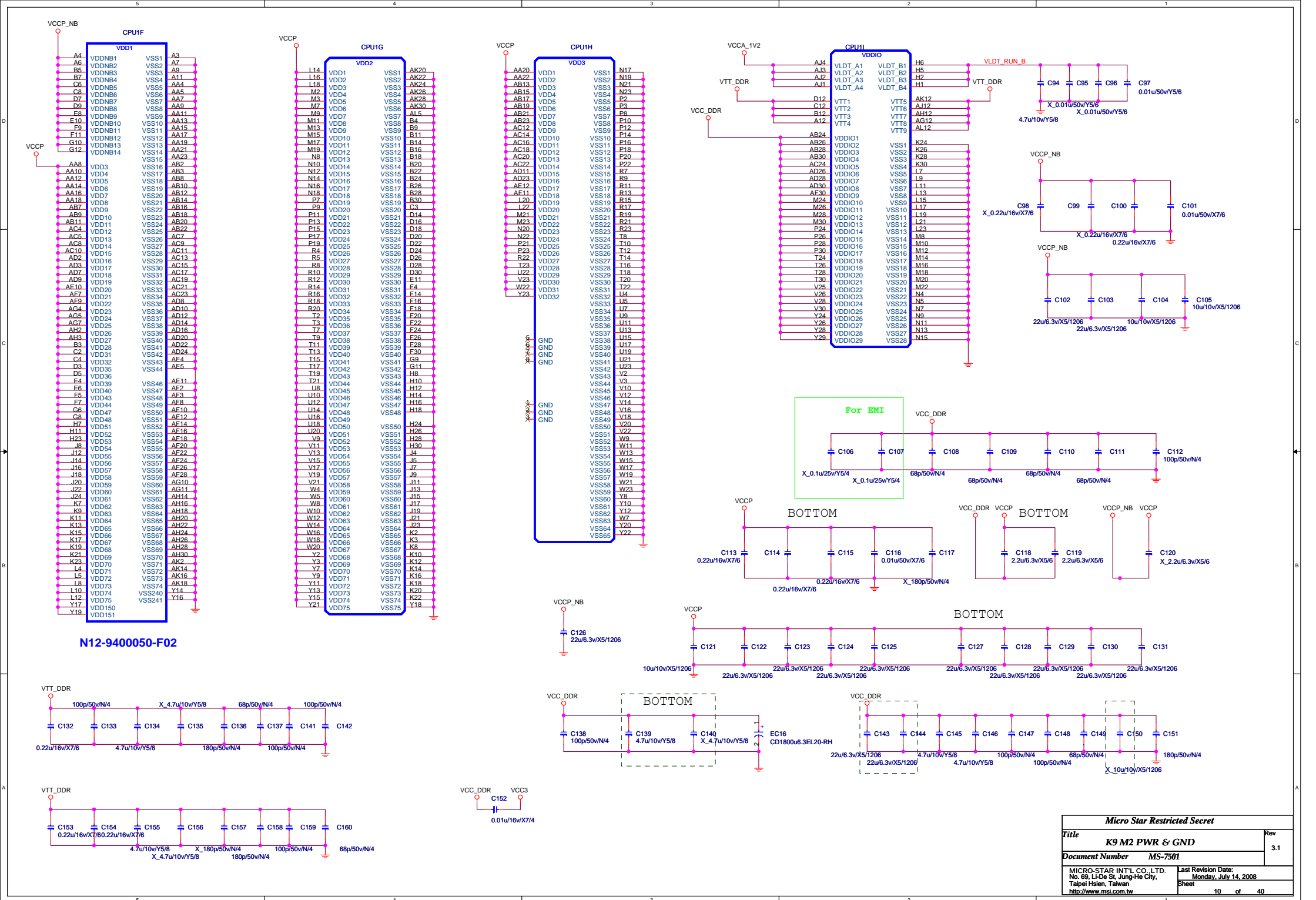
CPU1C

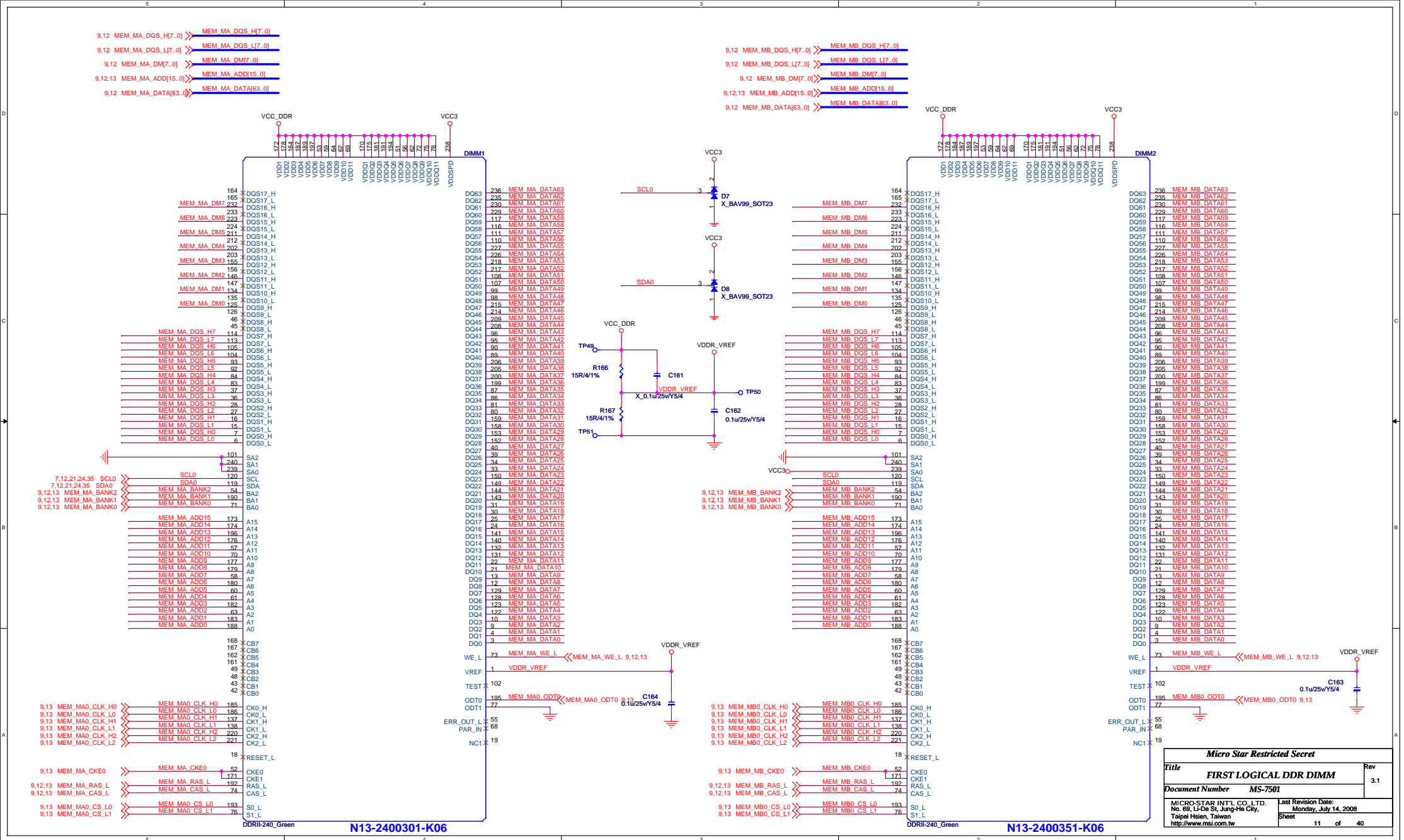
MEMORY INTERFACE B

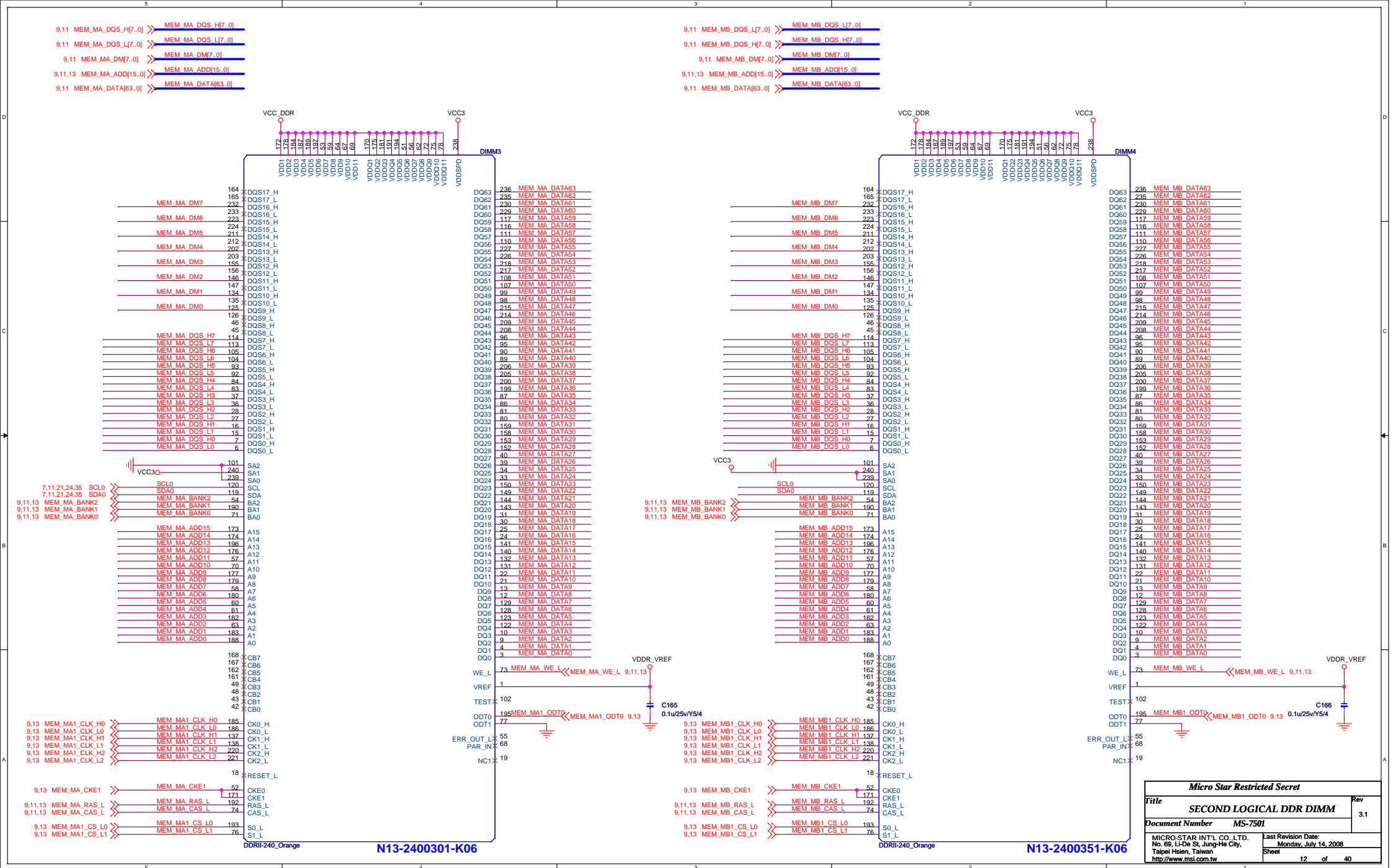
11,13 MEM_MB0_CLK_H2	>>	MEM_MB0_CLK_H2	AJ19	MB0_CLK_H(2)	MB_DATA(63)
11,13 MEM_MB0_CLK_L2	>>	MEM_MB0_CLK_L2	AK19	MB0_CLK_L(2)	MB_DATA(62)
11,13 MEM_MB0_CLK_H1	>>	MEM_MB0_CLK_H1	A18	MB0_CLK_H(1)	MB_DATA(61)
11,13 MEM_MB0_CLK_L1	>>	MEM_MB0_CLK_L1	A19	MB0_CLK_L(1)	MB_DATA(60)
11,13 MEM_MB0_CLK_H0	>>	MEM_MB0_CLK_H0	U31	MB0_CLK_H(0)	MB_DATA(59)
11,13 MEM_MB0_CLK_L0	>>	MEM_MB0_CLK_L0	U30	MB0_CLK_L(0)	MB_DATA(58)
11,13 MEM_MB0_CS_L1	>>	MEM_MB0_CS_L1	AE30	MB0_CS_L(1)	MB_DATA(57)
11,13 MEM_MB0_CS_L0	>>	MEM_MB0_CS_L0	AC31	MB0_CS_L(0)	MB_DATA(56)
11,13 MEM_MB0_ODT0	>>	MEM_MB0_ODT0	AD29	MB0_ODT(0)	MB_DATA(55)
12,13 MEM_MB1_CLK_H2	>>	MEM_MB1_CLK_H2	AL19	MB1_CLK_H(2)	MB_DATA(54)
12,13 MEM_MB1_CLK_L2	>>	MEM_MB1_CLK_L2	AL18	MB1_CLK_L(2)	MB_DATA(53)
12,13 MEM_MB1_CLK_H1	>>	MEM_MB1_CLK_H1	C18	MB1_CLK_H(1)	MB_DATA(52)
12,13 MEM_MB1_CLK_L1	>>	MEM_MB1_CLK_L1	D19	MB1_CLK_L(1)	MB_DATA(51)
12,13 MEM_MB1_CLK_H0	>>	MEM_MB1_CLK_H0	W29	MB1_CLK_H(0)	MB_DATA(50)
12,13 MEM_MB1_CLK_L0	>>	MEM_MB1_CLK_L0	W28	MB1_CLK_L(0)	MB_DATA(49)
12,13 MEM_MB1_CS_L1	>>	MEM_MB1_CS_L1	AE29	MB1_CS_L(1)	MB_DATA(48)
12,13 MEM_MB1_CS_L0	>>	MEM_MB1_CS_L0	AB31	MB1_CS_L(0)	MB_DATA(47)
12,13 MEM_MB1_ODT0	>>	MEM_MB1_ODT0	AD31	MB1_ODT(0)	MB_DATA(46)
11,12,13 MEM_MB_CAS_L	>>	MEM_MB_CAS_L	AC29	MB_CAS_L	MB_DATA(45)
11,12,13 MEM_MB_WE_L	>>	MEM_MB_WE_L	AC30	MB_WE_L	MB_DATA(44)
11,12,13 MEM_MB_RAS_L	>>	MEM_MB_RAS_L	AB29	MB_RAS_L	MB_DATA(43)
11,12,13 MEM_MB_BANK2	>>	MEM_MB_BANK2	N31	MB_BANK(2)	MB_DATA(42)
11,12,13 MEM_MB_BANK1	>>	MEM_MB_BANK1	AA31	MB_BANK(1)	MB_DATA(41)
11,12,13 MEM_MB_BANK0	>>	MEM_MB_BANK0	AA28	MB_BANK(0)	MB_DATA(40)
12,13 MEM_MB_CKE1	>>	MEM_MB_CKE1	M31	MB_CKE(1)	MB_DATA(39)
11,13 MEM_MB_CKE0	>>	MEM_MB_CKE0	M29	MB_CKE(0)	MB_DATA(38)
MEM_MB_ADD15	>>	MEM_MB_ADD15	N28	MB_ADD(15)	MB_DATA(37)
MEM_MB_ADD14	>>	MEM_MB_ADD14	N29	MB_ADD(14)	MB_DATA(36)
MEM_MB_ADD13	>>	MEM_MB_ADD13	AE31	MB_ADD(13)	MB_DATA(35)
MEM_MB_ADD12	>>	MEM_MB_ADD12	N30	MB_ADD(12)	MB_DATA(34)
MEM_MB_ADD11	>>	MEM_MB_ADD11	P29	MB_ADD(11)	MB_DATA(33)
MEM_MB_ADD10	>>	MEM_MB_ADD10	AA29	MB_ADD(10)	MB_DATA(32)
MEM_MB_ADD9	>>	MEM_MB_ADD9	P31	MB_ADD(9)	MB_DATA(31)
MEM_MB_ADD8	>>	MEM_MB_ADD8	R29	MB_ADD(8)	MB_DATA(30)
MEM_MB_ADD7	>>	MEM_MB_ADD7	R28	MB_ADD(7)	MB_DATA(29)
MEM_MB_ADD6	>>	MEM_MB_ADD6	R31	MB_ADD(6)	MB_DATA(28)
MEM_MB_ADD5	>>	MEM_MB_ADD5	R30	MB_ADD(5)	MB_DATA(27)
MEM_MB_ADD4	>>	MEM_MB_ADD4	T31	MB_ADD(4)	MB_DATA(26)
MEM_MB_ADD3	>>	MEM_MB_ADD3	T29	MB_ADD(3)	MB_DATA(25)
MEM_MB_ADD2	>>	MEM_MB_ADD2	U29	MB_ADD(2)	MB_DATA(24)
MEM_MB_ADD1	>>	MEM_MB_ADD1	U28	MB_ADD(1)	MB_DATA(23)
MEM_MB_ADD0	>>	MEM_MB_ADD0	AA30	MB_ADD(0)	MB_DATA(22)
MEM_MB_DQS_H7	>>	MEM_MB_DQS_H7	AK13	MB_DQS_H(7)	MB_DATA(21)
MEM_MB_DQS_L7	>>	MEM_MB_DQS_L7	AJ13	MB_DQS_L(7)	MB_DATA(20)
MEM_MB_DQS_H6	>>	MEM_MB_DQS_H6	AK17	MB_DQS_H(6)	MB_DATA(19)
MEM_MB_DQS_L6	>>	MEM_MB_DQS_L6	AJ17	MB_DQS_L(6)	MB_DATA(18)
MEM_MB_DQS_H5	>>	MEM_MB_DQS_H5	AK23	MB_DQS_H(5)	MB_DATA(17)
MEM_MB_DQS_L5	>>	MEM_MB_DQS_L5	AL23	MB_DQS_L(5)	MB_DATA(16)
MEM_MB_DQS_H4	>>	MEM_MB_DQS_H4	AL28	MB_DQS_H(4)	MB_DATA(15)
MEM_MB_DQS_L4	>>	MEM_MB_DQS_L4	AL29	MB_DQS_L(4)	MB_DATA(14)
MEM_MB_DQS_H3	>>	MEM_MB_DQS_H3	D31	MB_DQS_H(3)	MB_DATA(13)
MEM_MB_DQS_L3	>>	MEM_MB_DQS_L3	C31	MB_DQS_L(3)	MB_DATA(12)
MEM_MB_DQS_H2	>>	MEM_MB_DQS_H2	C24	MB_DQS_H(2)	MB_DATA(11)
MEM_MB_DQS_L2	>>	MEM_MB_DQS_L2	D17	MB_DQS_L(2)	MB_DATA(10)
MEM_MB_DQS_H1	>>	MEM_MB_DQS_H1	C17	MB_DQS_H(1)	MB_DATA(9)
MEM_MB_DQS_L1	>>	MEM_MB_DQS_L1	C17	MB_DQS_L(1)	MB_DATA(8)
MEM_MB_DQS_H0	>>	MEM_MB_DQS_H0	C14	MB_DQS_H(0)	MB_DATA(7)
MEM_MB_DQS_L0	>>	MEM_MB_DQS_L0	C13	MB_DQS_L(0)	MB_DATA(6)
MEM_MB_DM7	>>	MEM_MB_DM7	AJ14	MB_DM(7)	MB_DATA(5)
MEM_MB_DM6	>>	MEM_MB_DM6	AH17	MB_DM(6)	MB_DATA(4)
MEM_MB_DM5	>>	MEM_MB_DM5	AJ23	MB_DM(5)	MB_DATA(3)
MEM_MB_DM4	>>	MEM_MB_DM4	AK29	MB_DM(4)	MB_DATA(2)
MEM_MB_DM3	>>	MEM_MB_DM3	C30	MB_DM(3)	MB_DATA(1)
MEM_MB_DM2	>>	MEM_MB_DM2	A27	MB_DM(2)	MB_DATA(0)
MEM_MB_DM1	>>	MEM_MB_DM1	B17	MB_DM(1)	MB_CHECK(7)
MEM_MB_DM0	>>	MEM_MB_DM0	B13	MB_DM(0)	MB_CHECK(6)

Micro Star Restricted Secret

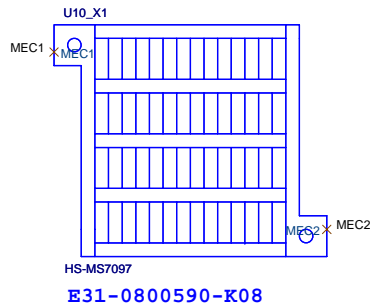
Title		Rev
K9 M2 DDR MEMORY I/F		3.1
Document Number		MS-7501
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Monday, July 14, 2008 Sheet
		9 of 40







NB HEAT-SINK



8 HT_CADOUT_H[15..0] >> HT_CADOUT_H[15..0]
8 HT_CADOUT_L[15..0] >> HT_CADOUT_L[15..0]

8 HT_CADIN_H[15..0] >> HT_CADIN_H[15..0]
8 HT_CADIN_L[15..0] >> HT_CADIN_L[15..0]

20 / 5 / 5 / 5 / 20

20 / 5 / 5 / 5 / 20

U10A
HT_CADOUT_H0 Y25
HT_CADOUT_L0 Y24
HT_CADOUT_H1 V22
HT_CADOUT_L1 V23
HT_CADOUT_H2 V25
HT_CADOUT_L2 V24
HT_CADOUT_H3 U24
HT_CADOUT_L3 U25
HT_CADOUT_H4 T25
HT_CADOUT_L4 T24
HT_CADOUT_H5 P22
HT_CADOUT_L5 P23
HT_CADOUT_H6 P25
HT_CADOUT_L6 P24
HT_CADOUT_H7 N24
HT_CADOUT_L7 N25
HT_CADOUT_H8 AC24
HT_CADOUT_L8 AC25
HT_CADOUT_H9 AB25
HT_CADOUT_L9 AB24
HT_CADOUT_H10 AA24
HT_CADOUT_L10 AA25
HT_CADOUT_H11 Y22
HT_CADOUT_L11 Y23
HT_CADOUT_H12 W21
HT_CADOUT_L12 W20
HT_CADOUT_H13 V21
HT_CADOUT_L13 V20
HT_CADOUT_H14 U20
HT_CADOUT_L14 U21
HT_CADOUT_H15 U19
HT_CADOUT_L15 U18

PART 1 OF 6

HYPER TRANSPORT CPU
I/F

HT_TXCAD0P D24
HT_TXCAD0N D25
HT_TXCAD1P E24
HT_TXCAD1N E25
HT_TXCAD2P F24
HT_TXCAD2N F25
HT_TXCAD3P F22
HT_TXCAD3N F23
HT_TXCAD4P H23
HT_TXCAD4N H22
HT_TXCAD5P J25
HT_TXCAD5N J24
HT_TXCAD6P K24
HT_TXCAD6N K25
HT_TXCAD7P K23
HT_TXCAD7N K22
HT_TXCAD8P G21
HT_TXCAD8N G20
HT_TXCAD9P H21
HT_TXCAD9N J20
HT_TXCAD10P J21
HT_TXCAD10N J18
HT_TXCAD11P K17
HT_TXCAD11N L19
HT_TXCAD12P L18
HT_TXCAD12N M19
HT_TXCAD13P L18
HT_TXCAD13N M21
HT_TXCAD14P P21
HT_TXCAD14N P18
HT_TXCAD15P M18
HT_TXCAD15N M18

8 HT_CLKOUT_H0 >>
8 HT_CLKOUT_L0 >>
8 HT_CLKOUT_H1 >>
8 HT_CLKOUT_L1 >>
8 HT_CTLOUT_H0 >>
8 HT_CTLOUT_L0 >>
8 HT_CTLOUT_H1 >>
8 HT_CTLOUT_L1 >>

T22 HT_RXCLK0P
AB23 HT_RXCLK0N
AA22 HT_RXCLK1P
HT_RXCLK1N
M22 HT_RXCTL0P
M23 HT_RXCTL0N
R21 HT_RXCTL1P
R20 HT_RXCTL1N

301R/4/1% R172 HT_RXCALP
HT_RXCALN A24

5 / 10

H24 HT_TXCLK0P
H25 HT_TXCLK0N
L21 HT_TXCLK1P
L20 HT_TXCLK1N
M24 HT_TXCTL0P
M25 HT_TXCTL0N
P19 HT_TXCTL1P
R18 HT_TXCTL1N

8 HT_CLKIN_H0 >>
8 HT_CLKIN_L0 >>
8 HT_CLKIN_H1 >>
8 HT_CLKIN_L1 >>
8 HT_CTLIN_H0 >>
8 HT_CTLIN_L0 >>
8 HT_CTLIN_H1 >>
8 HT_CTLIN_L1 >>

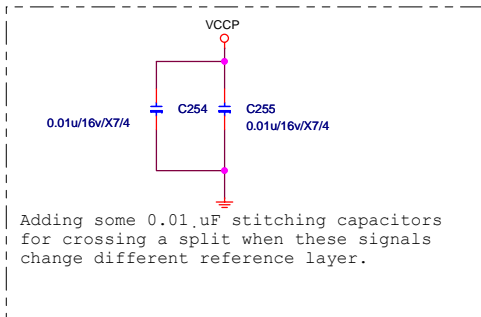
B24 HT_TXCALP
B25 HT_TXCALN

5 / 10

Check U10 New Version : Port Number

RX780/RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP	100R	1.21K	301R
HT_TXCALN			



MICRO-STAR IN'L CO., LTD.

Title			RS780-HT L
Size	Document Number	MS-7501	
Date:	Thursday, August 07, 2008	Sheet	14 of 40
			Rev 3.1

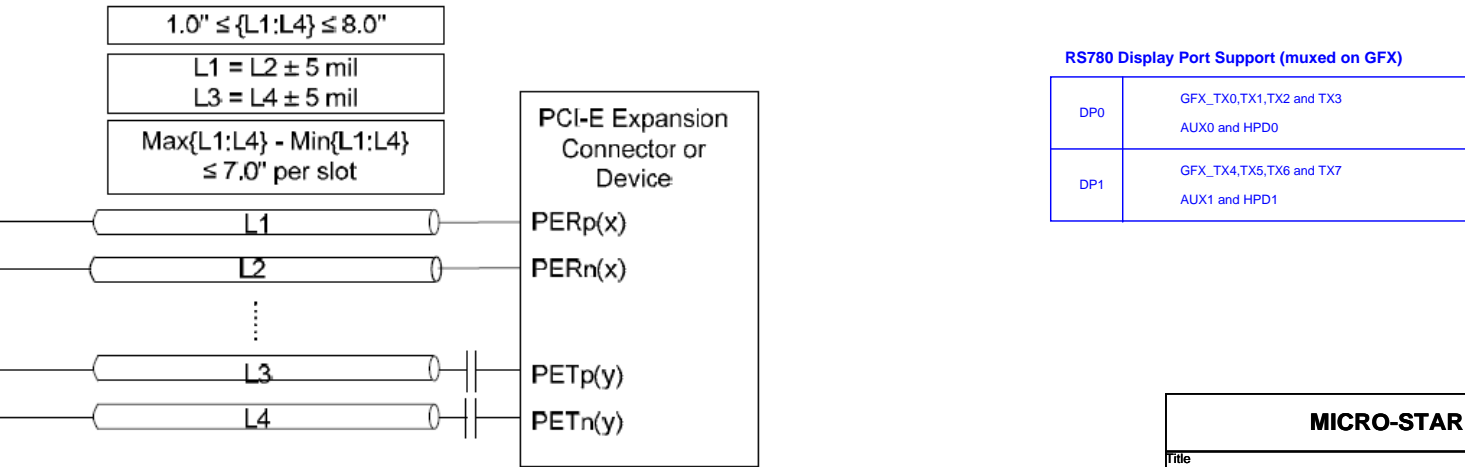
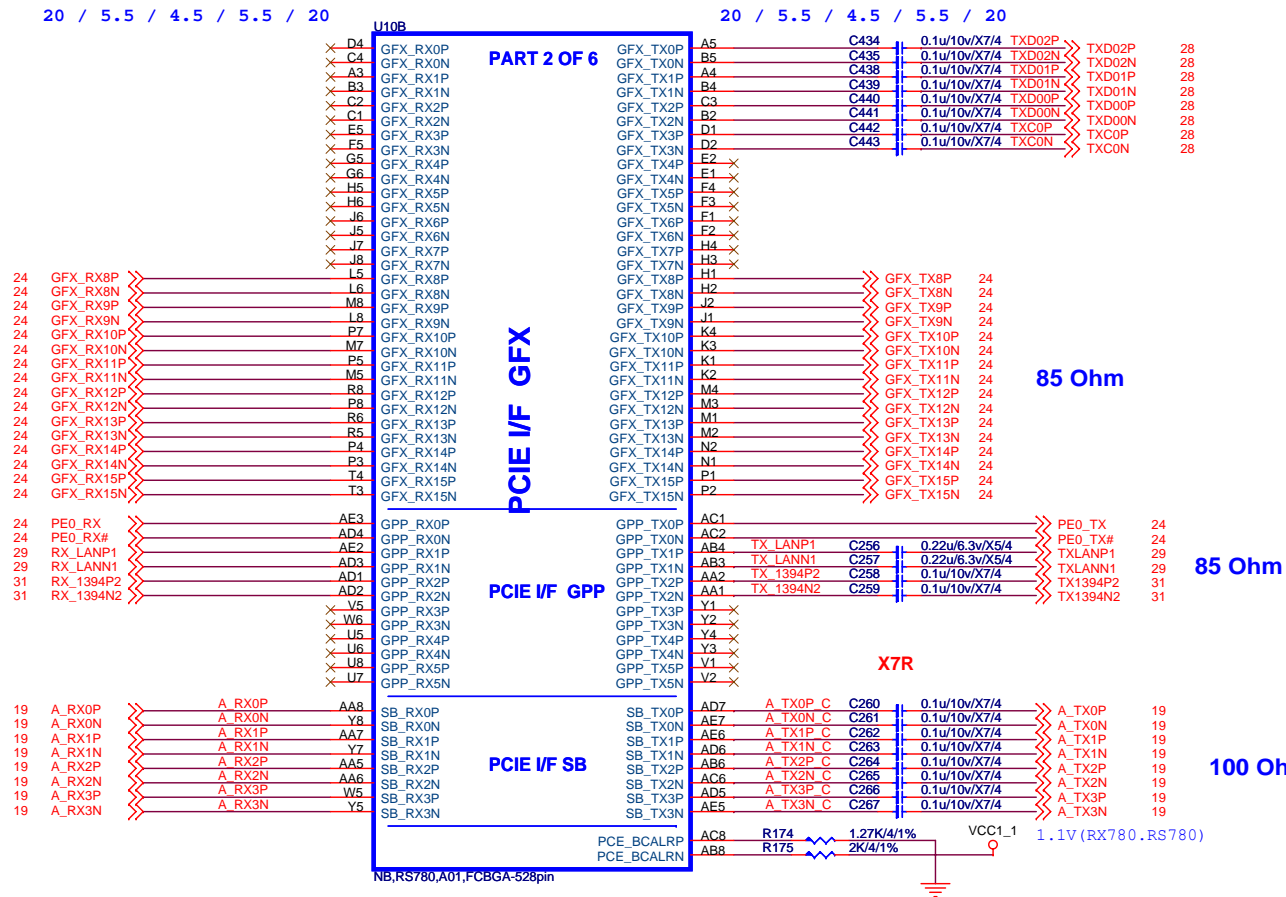
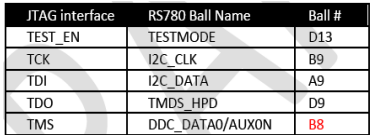
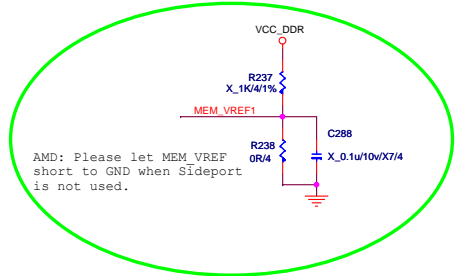
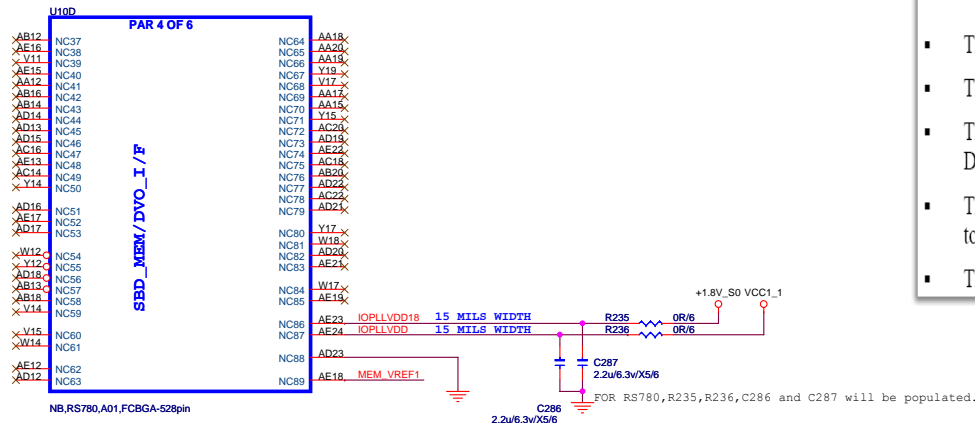


Figure 39: Layout Guidelines for the PCI-Express Expansion Interface



MICRO-STAR INT'L CO., LTD.			
Title			
RS780-SYSTEM I/F			
Size	Document Number		
	MS-7501		
Date:	Friday, July 25, 2008	Sheet	16 of 40

```
Enables Side port memory
1. Disable (RS740/RS780)
0 : Enable (RS740/RS780)
RS780: pin HSYNC
RX780: Not Applicable
```



- Note: If the Side-port memory interface is **not** used, make sure that:
- The memory interface IO power (VDD_MEM) is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
 - The memory interface IO transform power (VDD18_MEM) is connected to 1.8 V.
 - The voltage divider for memory interface reference voltage MEM_VREF is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
 - The memory interface PLL power IOPLLVD18 is connected to 1.8 V and IOPLLVD is connected to 1.2 V for the RS740 and to 1.1 V for the RS780.
 - The memory interface enable strap DFT_GPIO0 is **not** connected to the GND.

Max Power Estimates for RS780 and SB700

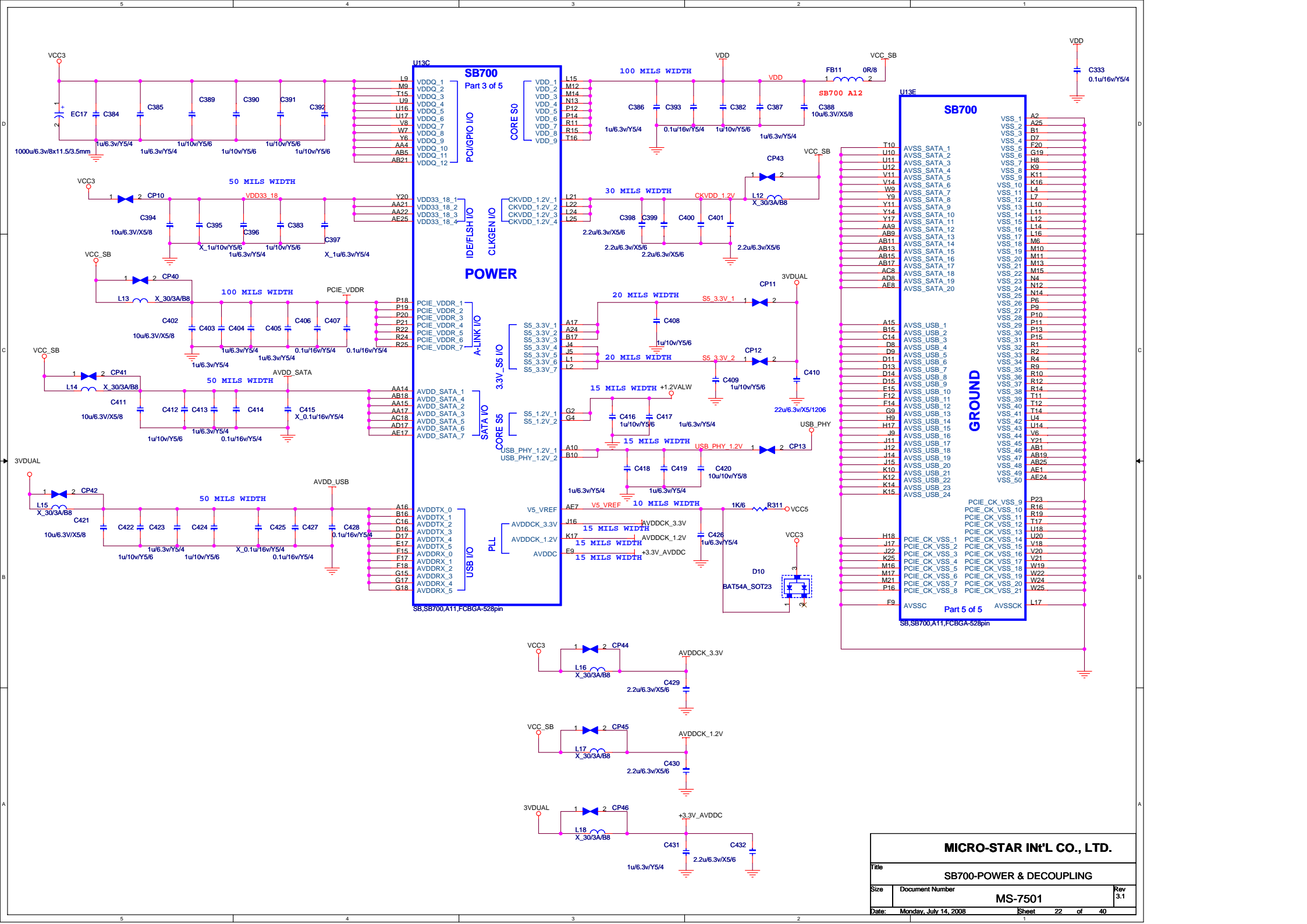
(Preliminary Data w/ Internal Clock Generator and IMC disabled) April 2007

Voltage	Usage	Domain	Max(Spec)
1.0-1.1V	RS780	S0/S1	10A
1.1V	RS780	S0/S1	3-4A
1.2V	RS780 & SB700	S0/S1	2.4A (1A-NB / 1.4A-SB)
1.8V	RS780& SB700	S0/S1	0.8A (0.75A-NB / 50mA-SB)

Max Power Estimates for RS780 and SB700 (continued)

April 2007

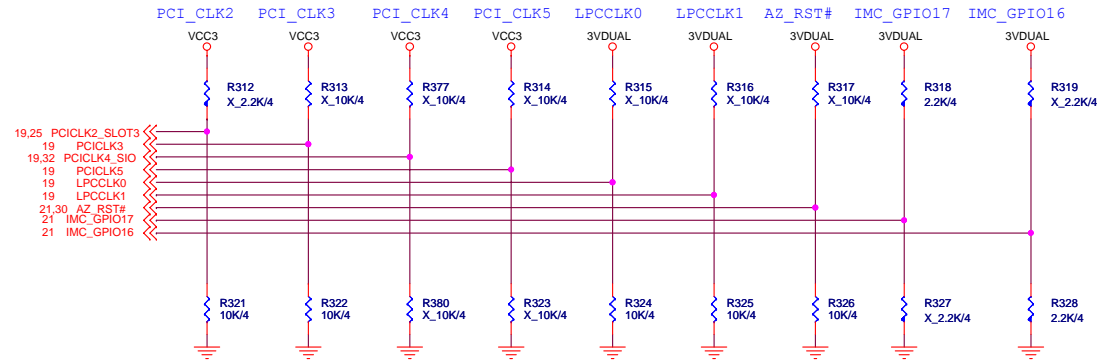
Voltage	Usage	Domain	Max(Spec)
3.3V	RS780& SB700	S0/S1	428mA (0.3A-NB / 128mA-SB)
1.2VDual	SB700	S0/S1/S2/S3/S4/S5	217mA
3.3VDual	SB700	S0/S1/S2/S3/S4/S5	495mA
5V	SB700 V5_VREF	S0/S1	0.21mA





REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17	IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	IMC ENABLED	ROM TYPE: H, H = Reserved H, L = SPI ROM	
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	IMC DISABLED DEFAULT	L, H = LPC ROM L, L = FWH ROM DEFAULT	

DEBUG STRAPS

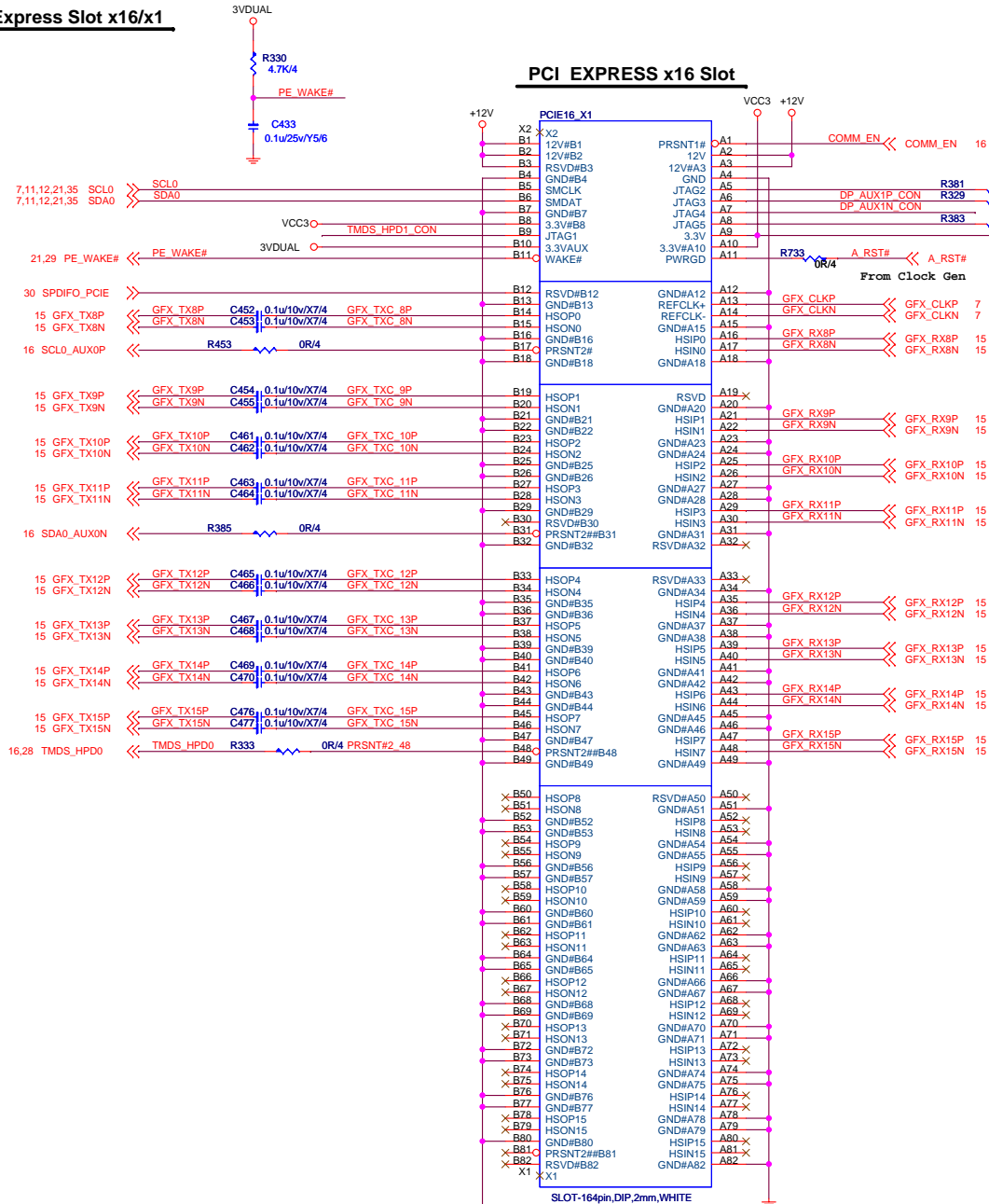
SB700 HAS 15K INTERNAL PU FOR PCI_AD[30:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

MICRO-STAR INT'L CO., LTD.

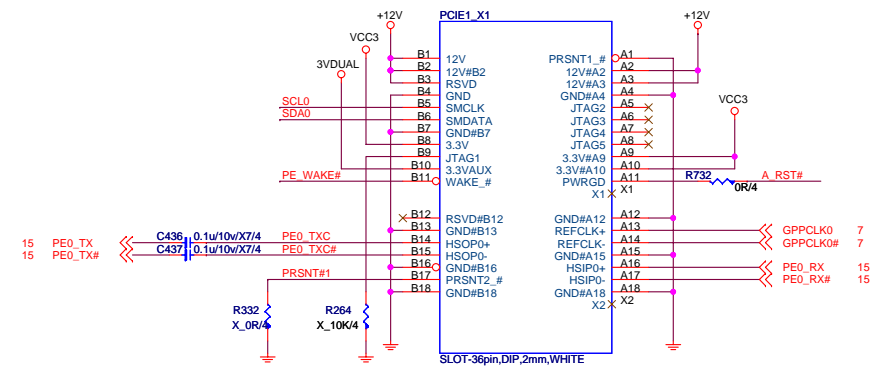
Title				SB700-STRAPS			
Size	Document Number						Rev
	MS-7501						3.1
Date:	Monday, July 14, 2008						Sheet
							23 of 40

PCI Express Slot x16/x1

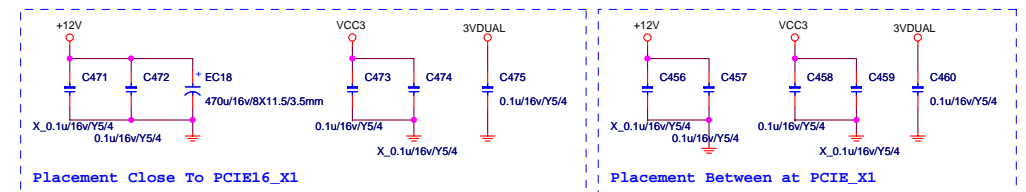


N11-1640401-K06

PCI EXPRESS 1 Slot-1



N11-0360091-F02

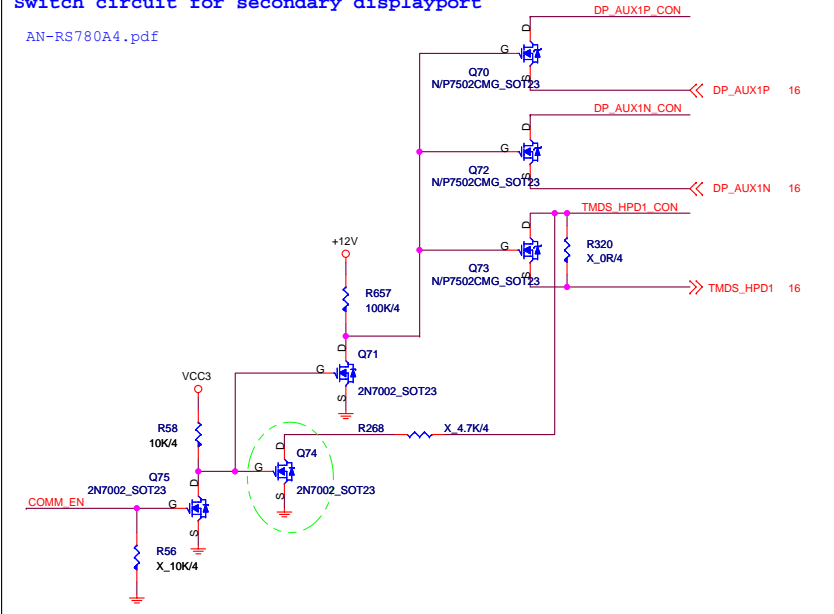


Placement Close To PCIE16_X1

Placement Between at PCIE_X1

Switch circuit for secondary displayport

AN-RS780A4.pdf

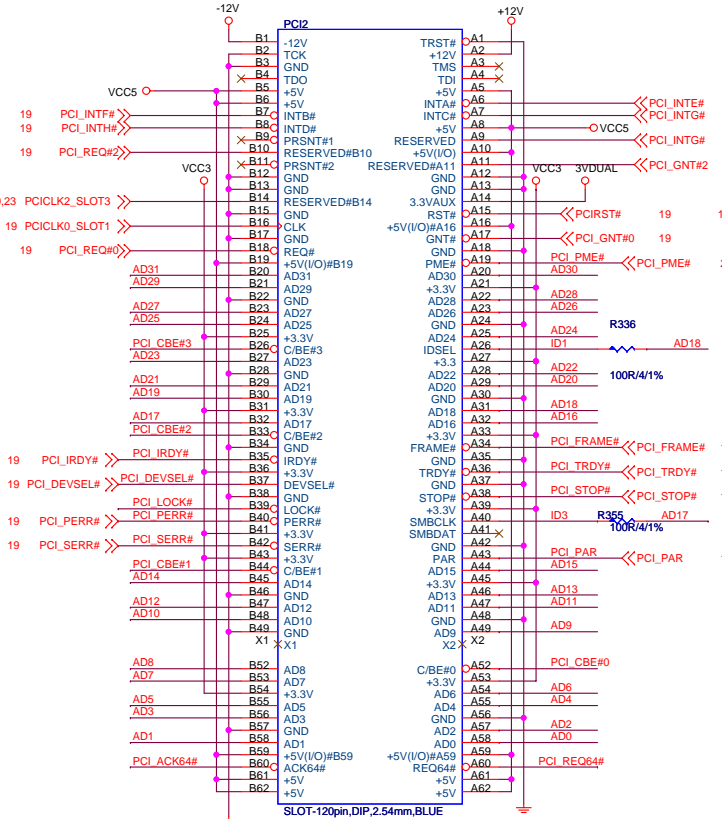


Title	PCI EXPRESS X16 & X1 SLOT
-------	---------------------------

Size	Document Number	Rev
Custom	MS-7501	3.1
Date:	Monday, July 14, 2008	Sheet 24 of 40

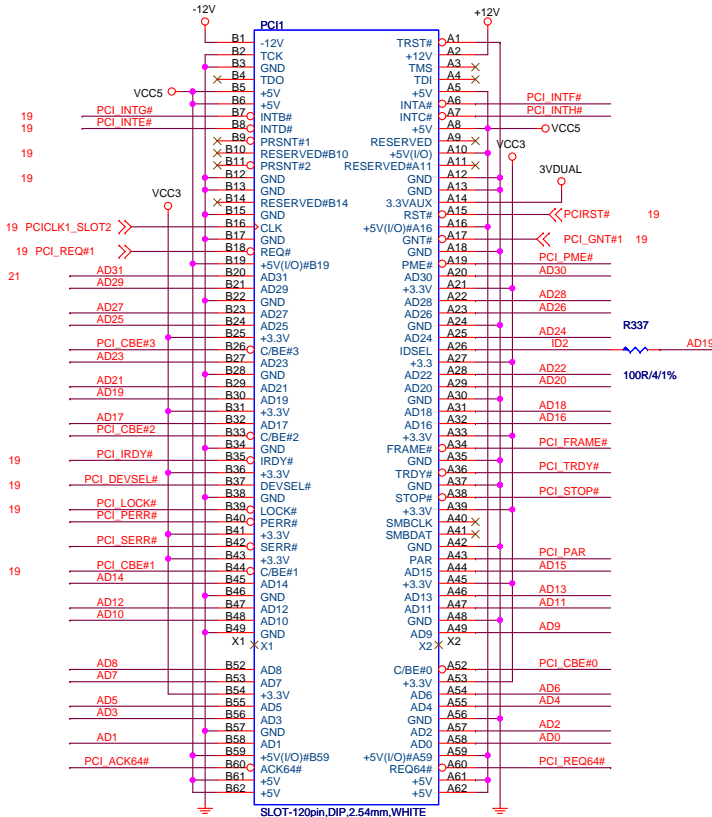
19 AD[31..0] >> AD[31..0]
19 PCI_CBE#[3..0] >> PCI_CBE#[3..0]

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

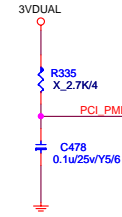


IDSEL = AD18
MASTER = PCI_REQ#2
PCI_GNT#0
PCI_GNT#2

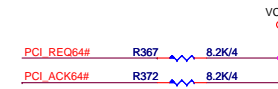
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



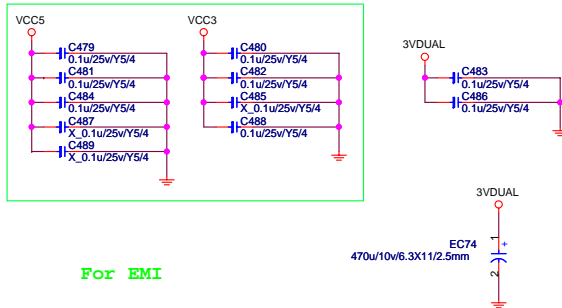
IDSEL = AD19
MASTER = PCI_REQ#1
PCI_GNT#1



PCI PULL UPS

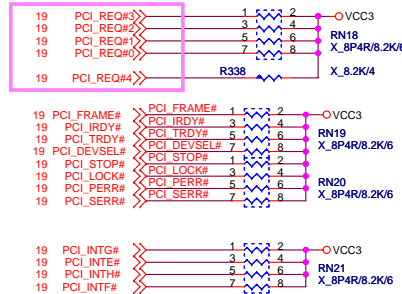


PCI SLOT DECOUPLING CAPACITORS



For EMI

PCI PULL-UP / DOWN RESISTORS

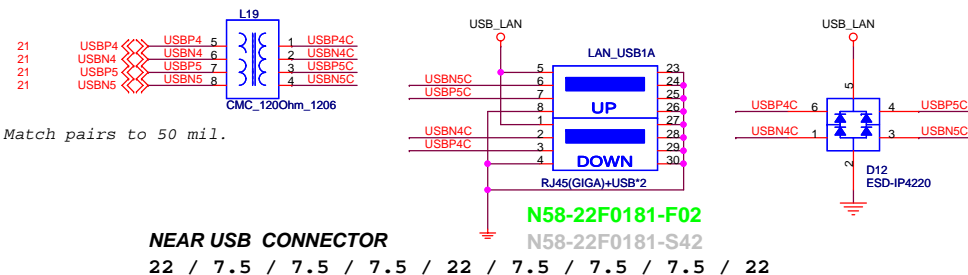


Micro Star Restricted Secret		
Title	PCI Slot 1 2	Rev
Document Number	MS-7501	3.1
MICRO-STAR INT'L CO., LTD. No. 68, Lihde St., Jung-Ho City, Taipei Hsien, Taiwan		
Last Revision Date:		Monday, July 14, 2008
Sheet		25 of 40

[illegible]

Part Number ? UP7533?

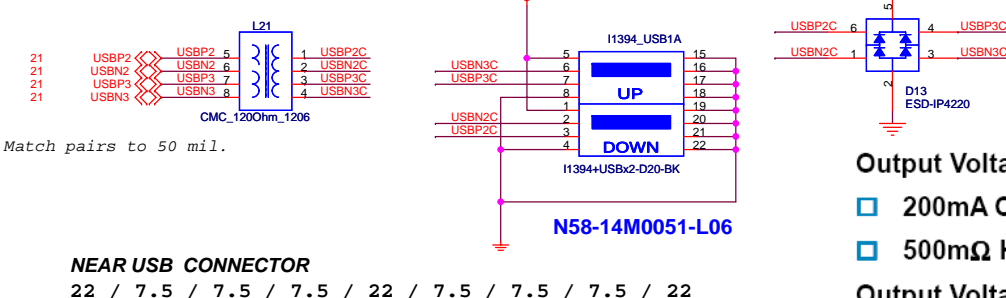
Trace lengths must be less 12 inches



NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

Trace lengths must be less 12 inches



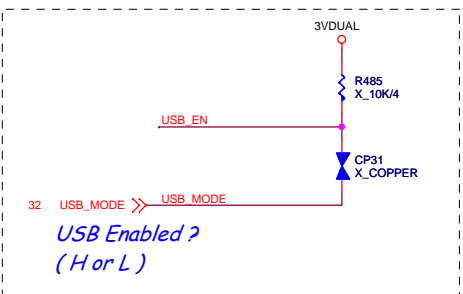
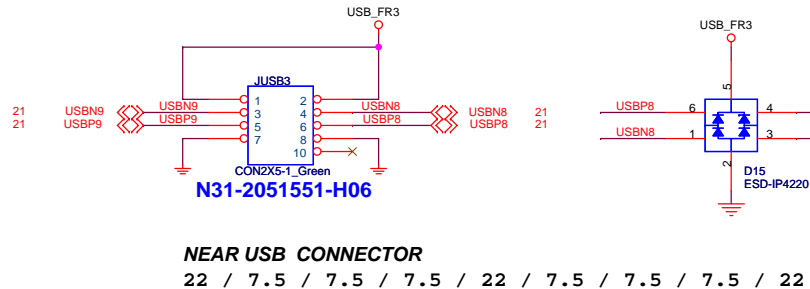
SB at S3/S4/S5 **N31-2051461-H06**

Current

NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 /

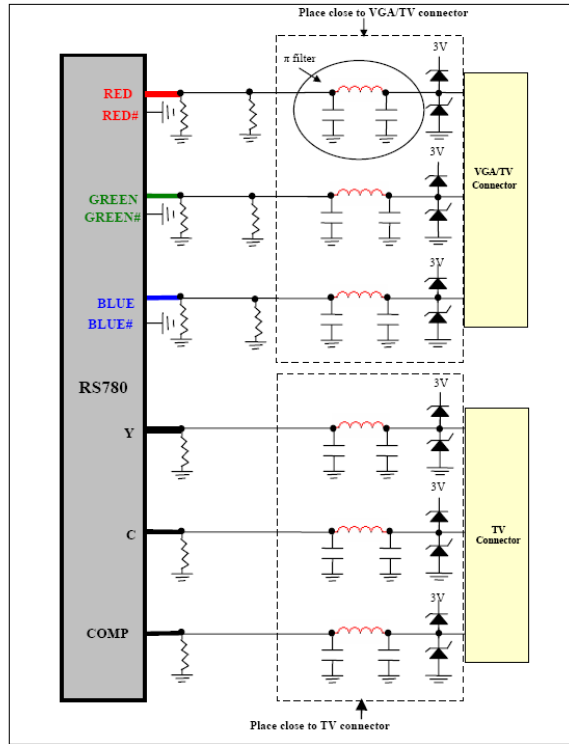
Trace lengths must be less 5 inches



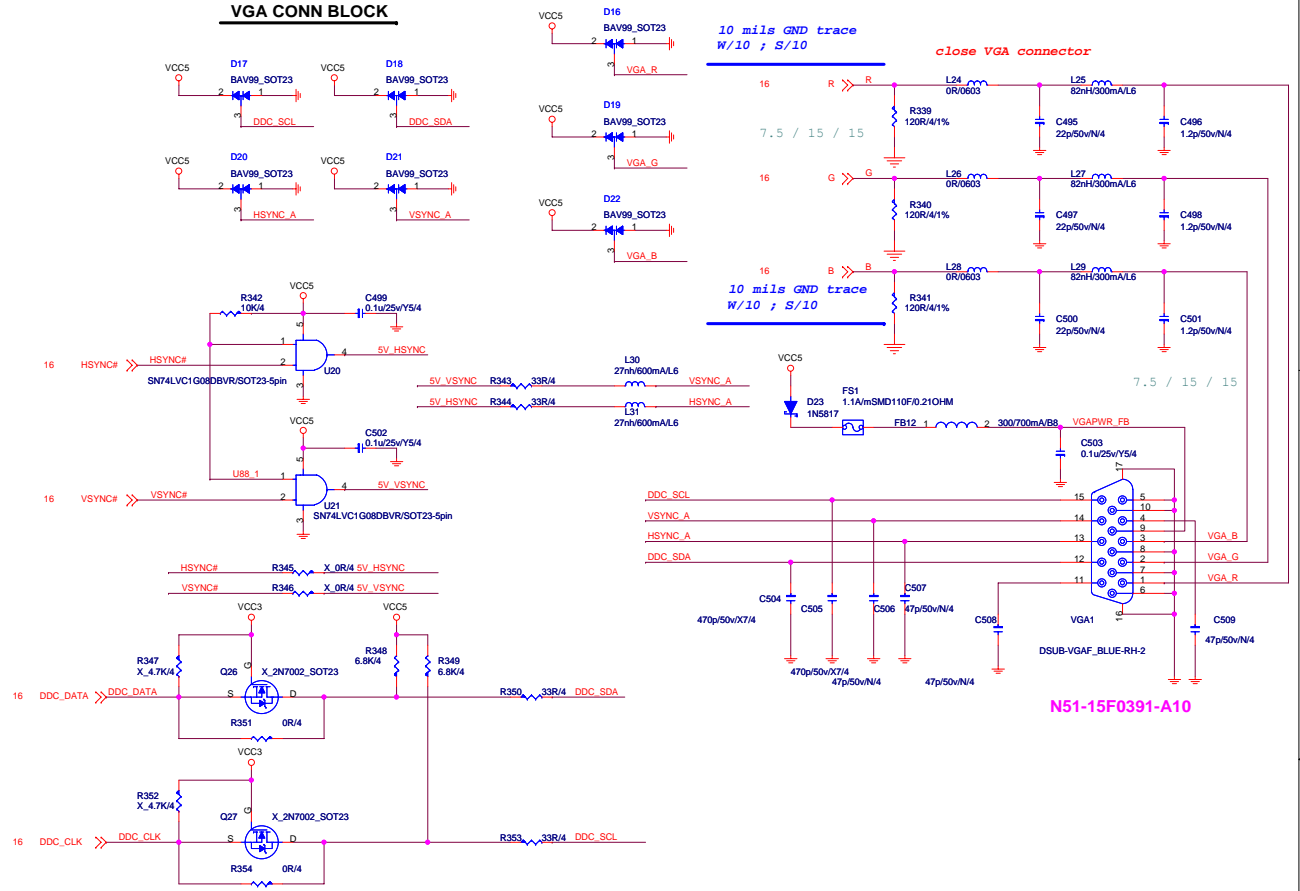
MICRO-STAR INT'L CO., LTD.

Title			
USB Conn.			
Size	Document Number	Rev	
	MS-7501	3.1	
Date:	Monday, July 14, 2008	Sheet	26 of 40

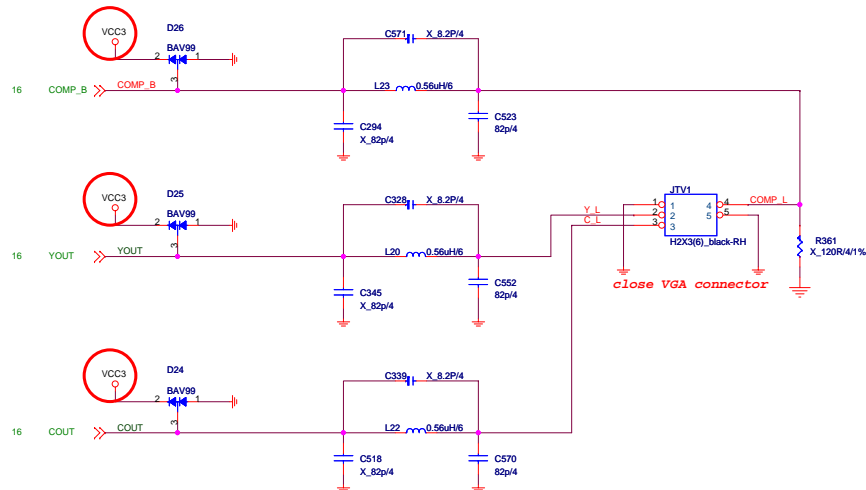
Figure 29: Placement of VGA and TV-Out Connectors



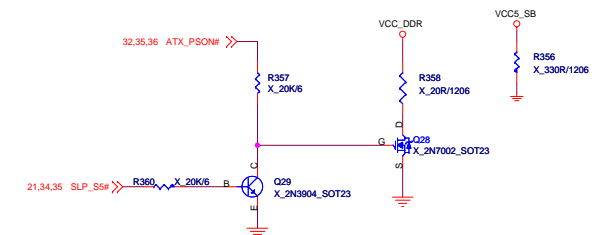
VGA CONN BLOCK



TV_OUT CONNECTOR



MEMORY VOLTAGE BLEED-OFF CIRCUIT



MICRO-STAR INT'L CO., LTD.

File	VGA CONN		
Size	Document Number	MS-7501	Rev 3.1
Date	Monday, July 21, 2008	Sheet 27 of 40	

15 / 5 / 7 / 5 / 15

HDMI CONNECTOR

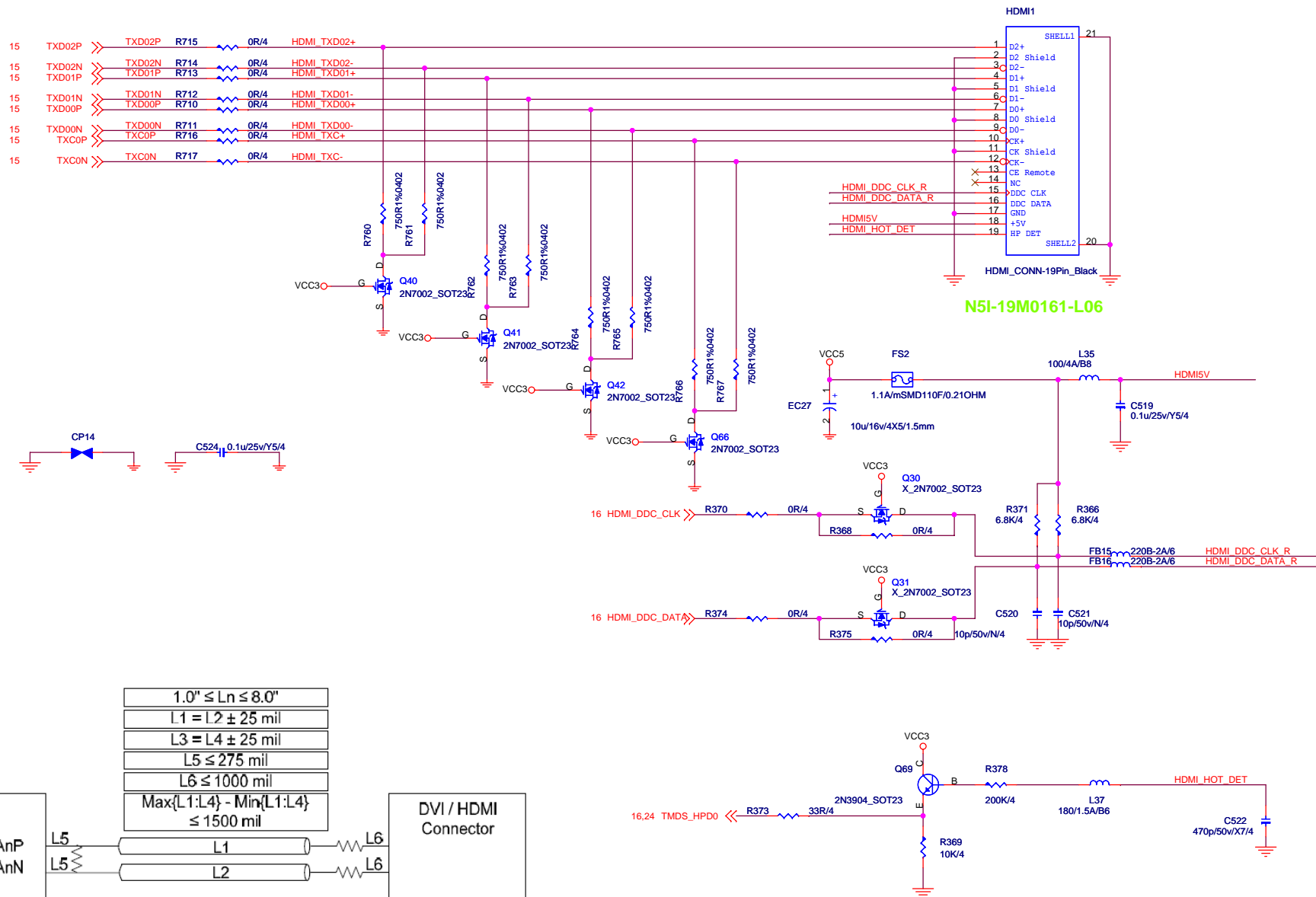
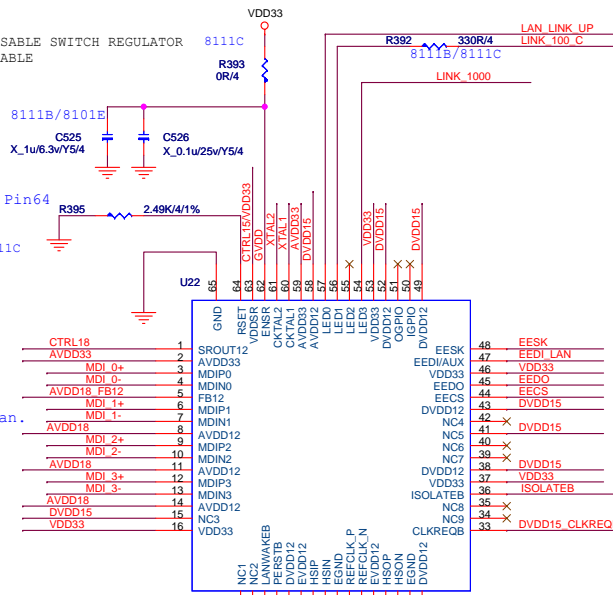


Figure 32: Layout Guidelines for the DVI/HDMI Signals

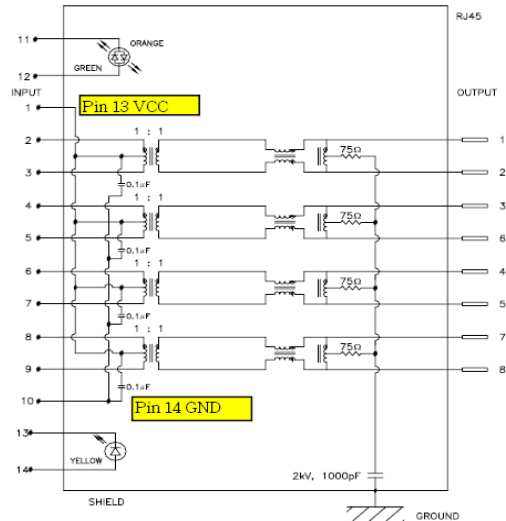
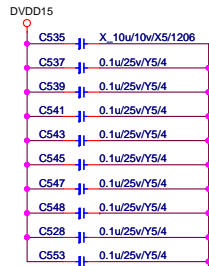
MICRO-STAR IN'L CO., LTD.

Title			HDMI CONNECTOR
Size	Document Number	MS-7501	
Date:	Wednesday, August 13, 2008	Sheet	28 of 40
		Rev	3.1

0 : DISABLE SWITCH REGULATOR
1 : ENABLE



MDI+/- Reference to GND plan.



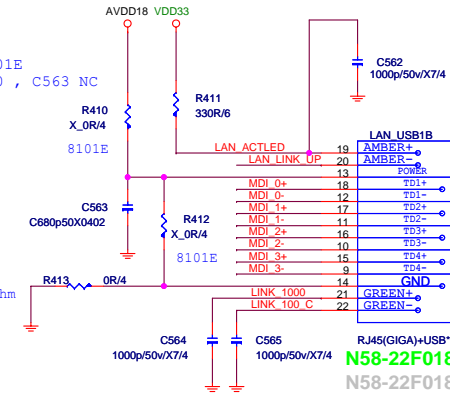
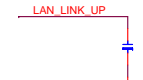
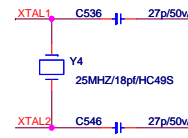
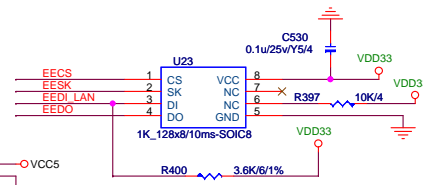
Power domain chart

	RTL8111B / RTL8101E	RTL8111C
AVDD33	3.3V	3.3V
AVDD18	1.8V	1.2V
EVDD18	1.8V	1.2V
DVDD15	1.5V	1.2V
RTL8111B	Need	Need
RTL8111C	N/A	N/A
RTL8101E	N/A	N/A

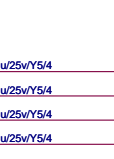
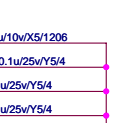
For RTL8101E stuff R410, C563 NC

8111B/8111C to 0 ohm
8101E to 0.01uF

- Pin 64: RSET res. should be close to LAN chip. Don't have power trace or high frequency trace beside it.
- The trace of each Pair (MDIX+/-) should be equal in length and better have ground under.
- RTL8111B/C/8101E, Pin 1~16 forward to transformer, this will make the trace more short.
- As the Layout Guide, the output pin of Transistor trace please layout it more widely.
- Make nine through holes at the center of IC board. The back side of IC is GND. Please be aware to connect this GND to the GND of outside of LAN chip.
- Both EGND and GND can be connect together or use 0 Ohm res. to connect them.
- The Spec of transistor suggest use the current least 1.2A.
- 1.5V請留 power plane並且盡量大一點.
- 1.5V Bypass 電容不能省. Add 0.1u cap. for each power pin of LAN.
- For RTL8111B, Pin62 有外接兩顆電容絕對不能省.



CHOKE7 close to U22 Pin 1 within 0.5cm



Power consumption			Giga-Lan		10/100-Lan	
	1G	100M	N58-22F0081-S42		N58-22F0061-S42 N58-22F0061-F02	
3.3V	103mA	TBD	Link	Yellow	Link	Yellow
1.5V	367mA	TBD	Active	Blinking	Active	Blinking
1.8V	198mA	TBD	1000	Orange	100	Green
			100	Green	10	None
			10	None		
19				Yellow	19	Yellow
20				Yellow	20	Yellow
21				Orange	21	Green
22				Green	22	Green

Micro Star Restricted Secret		
Title LAN - Realtek 8111C/8101E		
Document Number MS-7501		
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		
Last Revision Date: Monday, July 14, 2008		
Sheet 29 of 40		
Rev 3.1		

1394 CONTROLLER

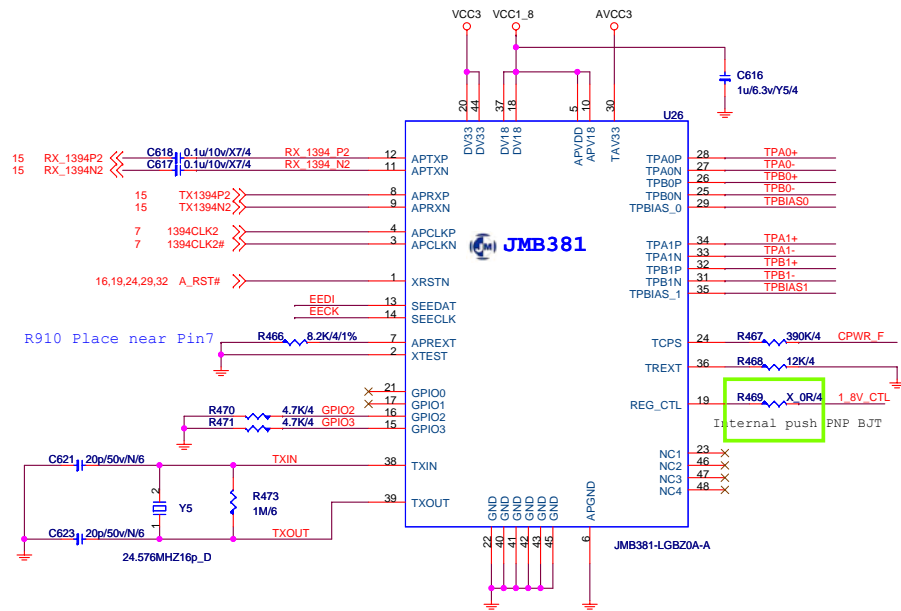
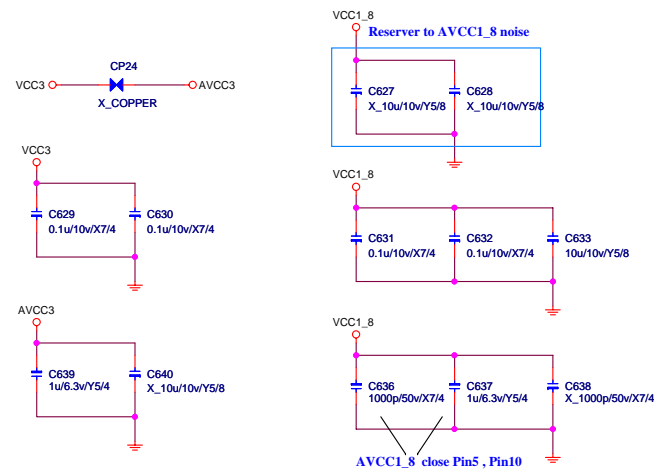
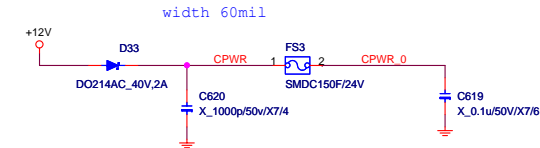
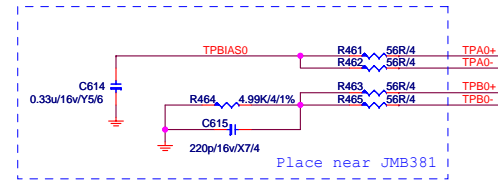


Table 5.1 JMB381 Operating Modes

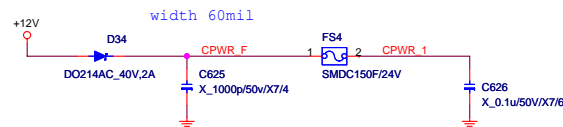
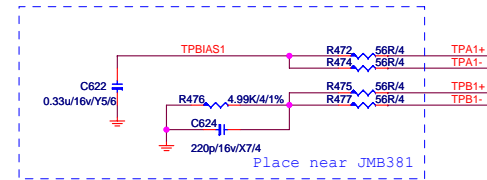
	Normal	IDDQ	BIST/FL	Nandtree
XTEST	0	1	1	1
GPIO2	x	0	0	1
GPIO3	x	0	1	1



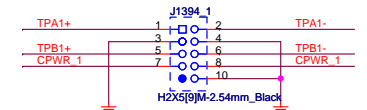
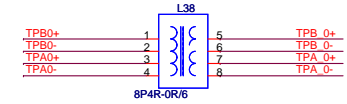
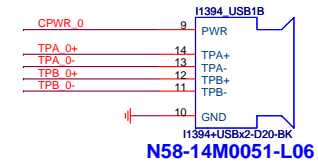
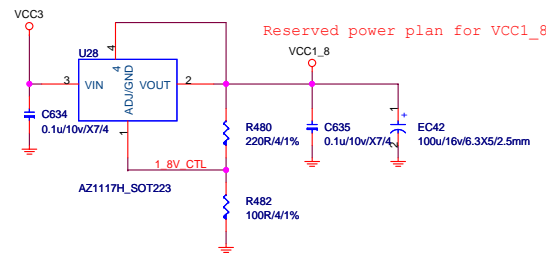
Rear 1394 port



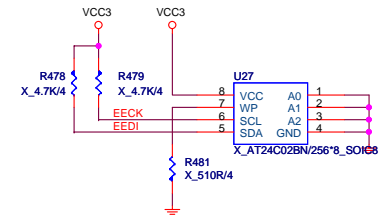
Front 1394 pin header



A1117 CO-LAY SOT223 (TO_261) PNP BJT



For Intel 1394 pinheader

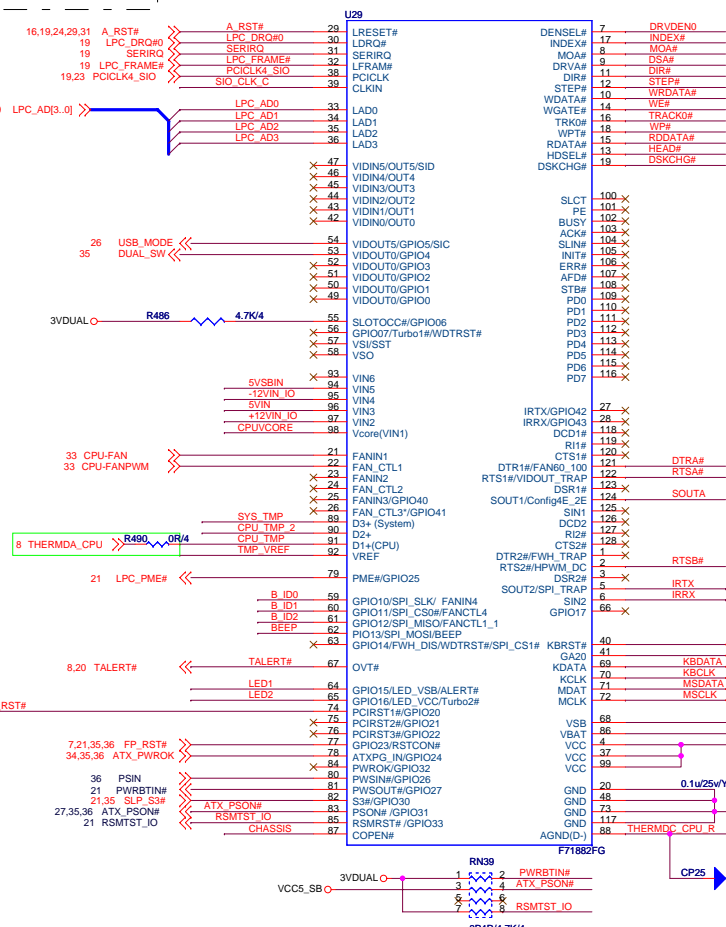


S3 Resume time

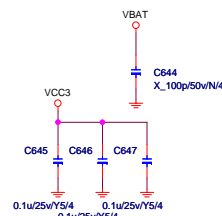
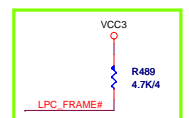
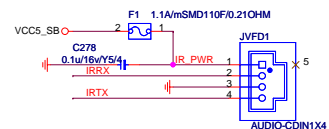
Title				
1394 Controller - JMB381				
Size	Document Number			Rev
	MS-7501			3.1
Date:	Wednesday, August 13, 2008	Sheet	31	of 40

Super I/O

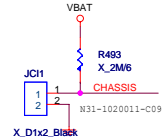
LPC SUPER I/O F71882



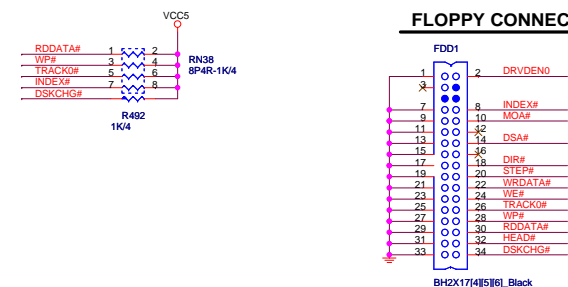
Front LCD (SERIAL PORT 2)



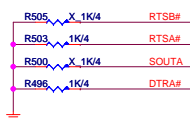
Chassis Intrusion



FLOPPY CONNECTOR

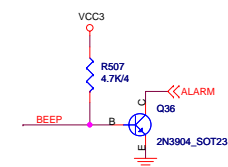


LPC I/O STRAPPING RESISTOR

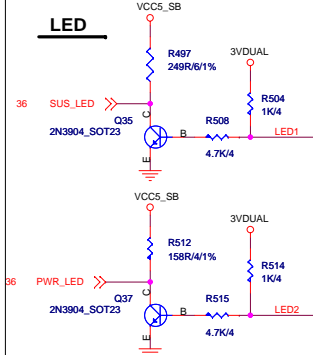


	Don't STUFF	STUFF
RTSB#	PWM FAN	LINEAR FAN
RTSA#	PIN49-54=VID_OUT PIN42-47=VIDIN	PIN49-54=GPIO PIN42-47=VIDIN/OUT
SOUTA	4E	2E
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%

BEEP

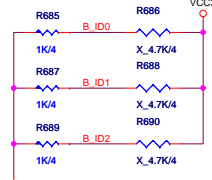


LED

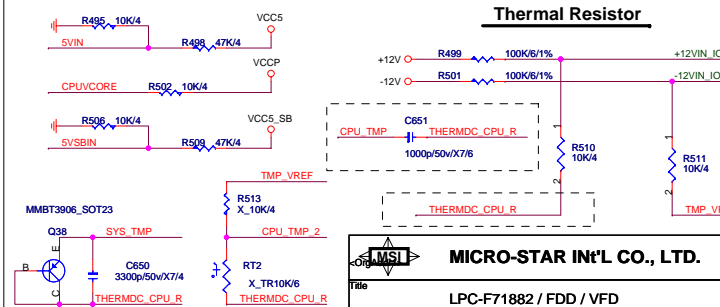


Board ID

Board ID [2:0]	Function
0 0 0	Normal
1 0 0	DOT?



Thermal Resistor



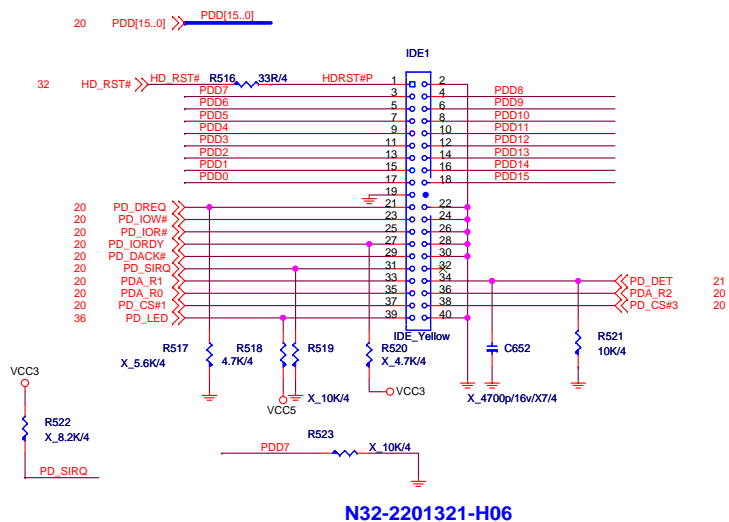
**NOTE: LOCATE CLOSE
STATUS PANEL**

 **MICRO-STAR INT'L CO., LTD.**

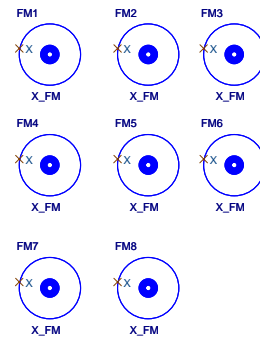
Title	LPC-F71882 / FDD / VFD
-------	------------------------

Size	Document Number	Rev
	MS-7501	3.1
Date:	Monday, July 14, 2008	Sheet 32 of 40

IDE 1



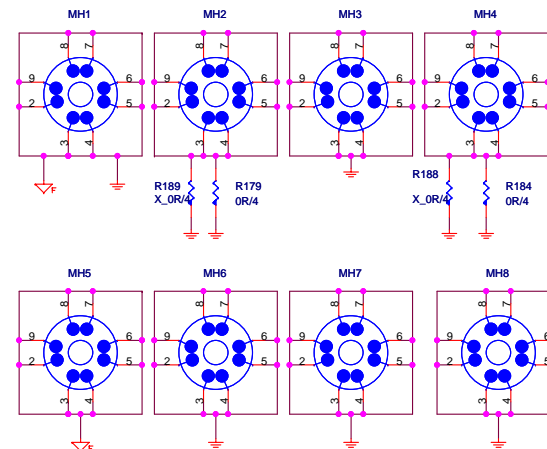
Optics Orientation Holes



Simulation

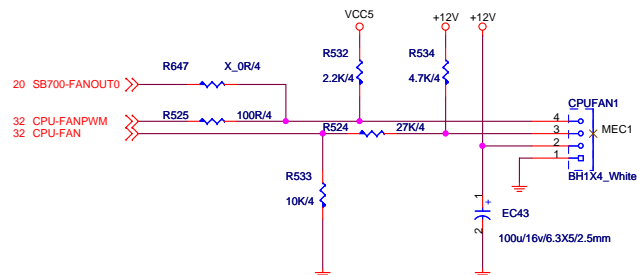


Mounting Holes



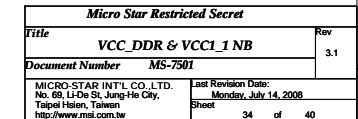
FAN CONTROL

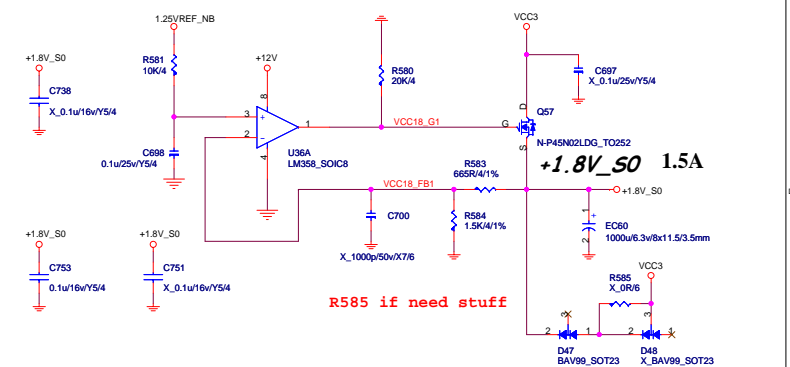
CPU FAN



Micro Star Restricted Secret

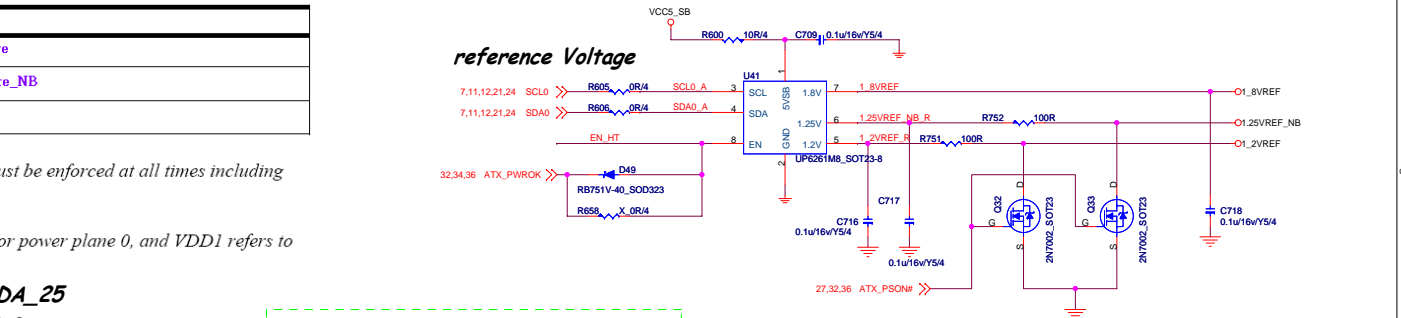
Title	Rev
IDE Conn / FAN	3.1
Document Number	MS-7501
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Wednesday, August 13, 2008 Sheet 33 of 40



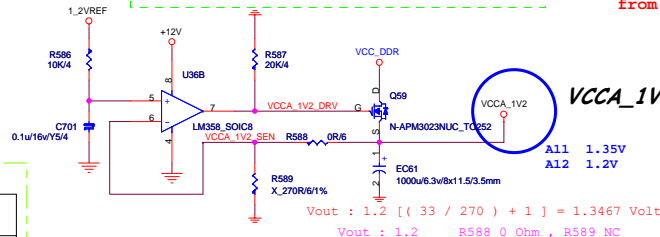


Power Group A	Power Group B
VDDIO ^{1,2} <i>Vcc_DDR</i>	VDD[1:0] ³ <i>Vcore</i>
VTT ^{1,2} <i>VTT</i>	VDDNB <i>Vcore_NB</i>
VDDA <i>VDDA25</i>	VLDT <i>HT</i>

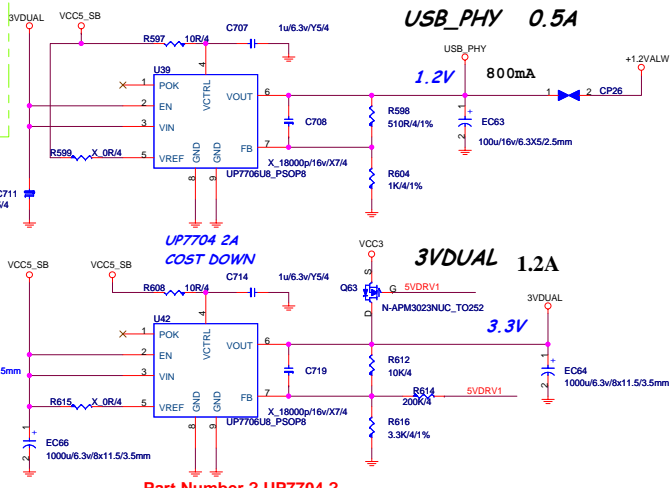
- 1) *VDDIO must never exceed VTT by greater than X.XX V. This relationship must be enforced at all times including power-up, power-down, and power failure.*
- 2) *VDDIO and VTT only apply to DDR2 compatible processors.*
- 3) *VDD refers generically to the core voltage plane(s). VDD0 refers to processor power plane 0, and VDD1 refers to processor power plane 1.*



ER_RS780A1.pdf
from 1.2V change to 1.35V



USB_PHY 0.5A

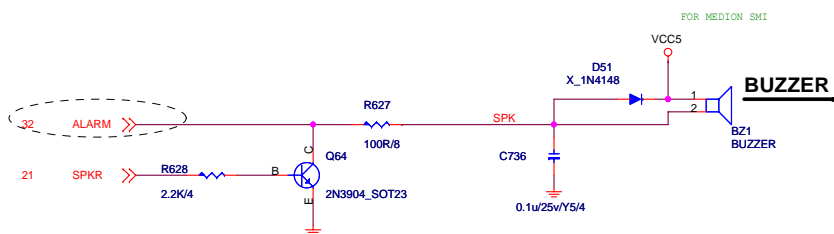
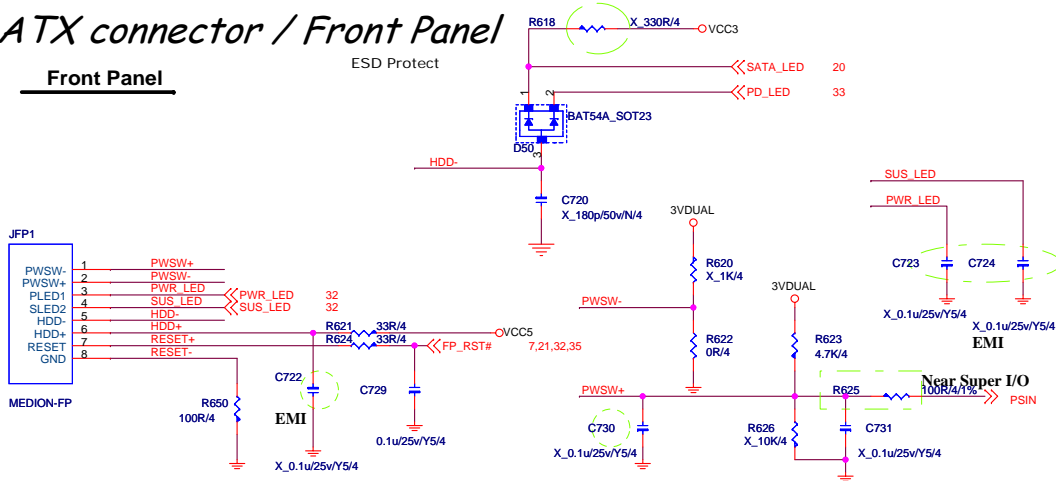
[illegible]

<i>Micro Star Restricted Secret</i>		
Title	ACPI by UPI	Rev
Document Number	MS-7501	3.1
MICRO-STAR INT'L CO., LTD. No. 68, Li-De St., Jung-Ho City, Taichung, Taiwan http://www.msi.com.tw		Last Revision Date: Wednesday, August 13, 2008 Sheet 35 of 40

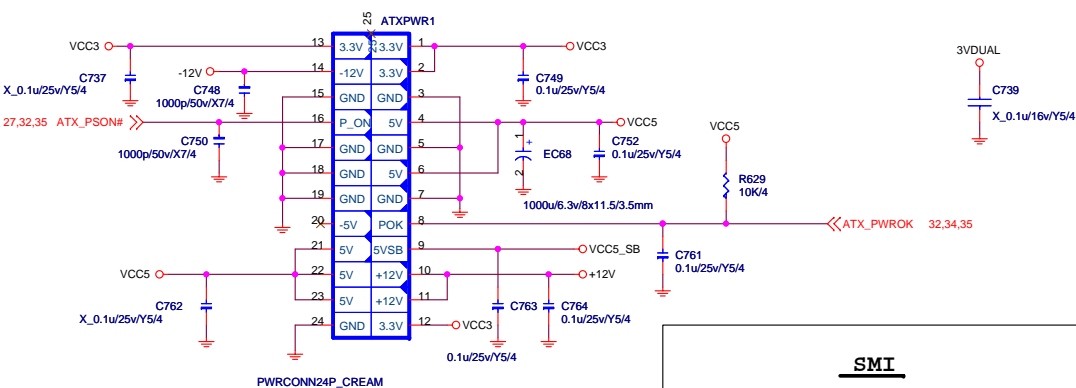
ATX connector / Front Panel

Front Panel

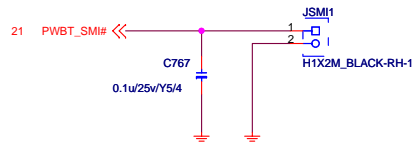
ESD Protect



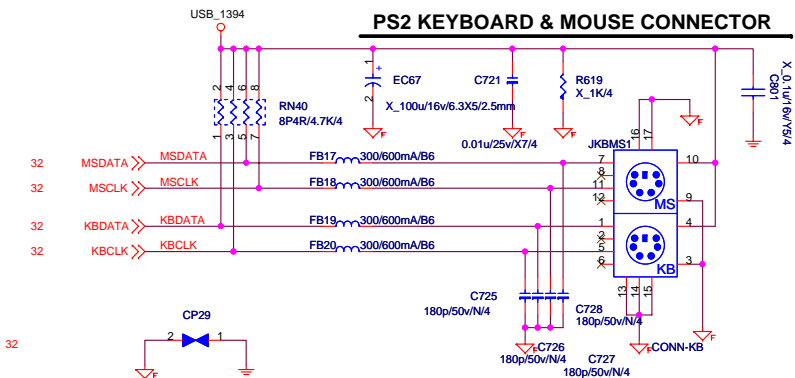
ATX Connector



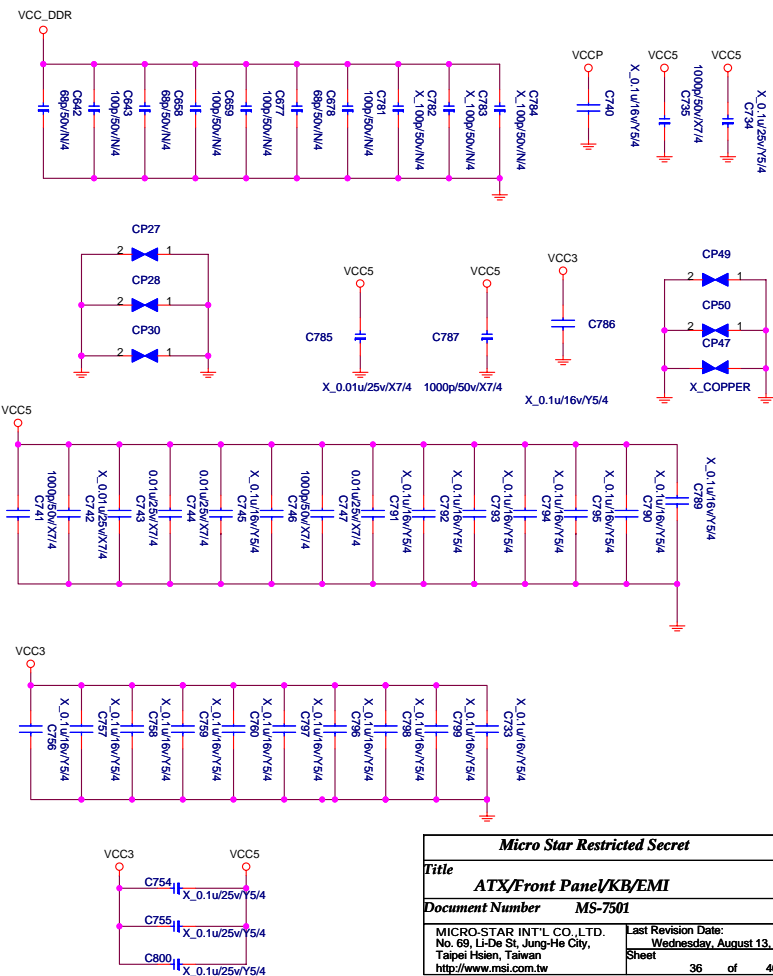
SMI



PS2 KEYBOARD & MOUSE CONNECTOR

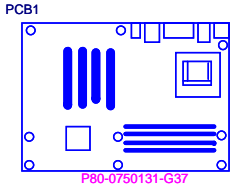


EMI solution



Micro Star Restricted Secret		
Title	ATX/Front Panel/KB/EMI	Rev 3.1
Document Number	MS-7501	
MICRO-STAR INT'L CO., LTD. No. 69, Li-Da St., Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Wednesday, August 13, 2008
Sheet		36 of 40

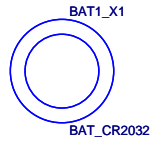
PCB



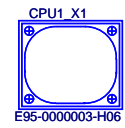
PCB : 2116

P80-0750131-G37
P80-0750131-E55

BATTERY



CPU RM

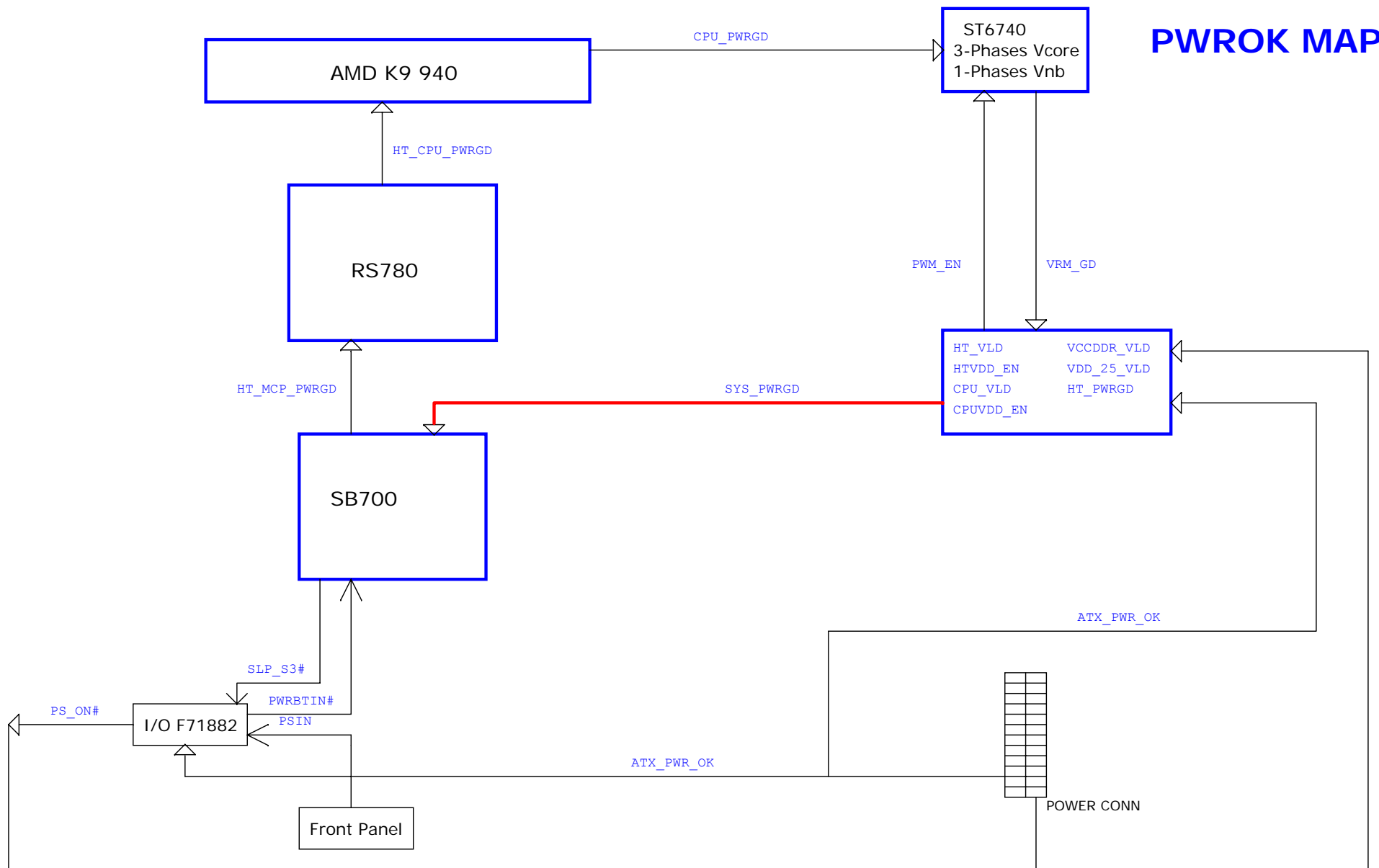


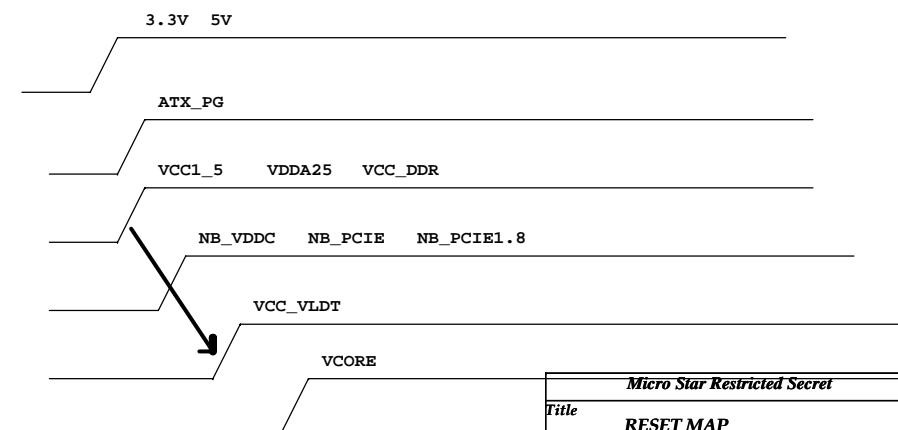
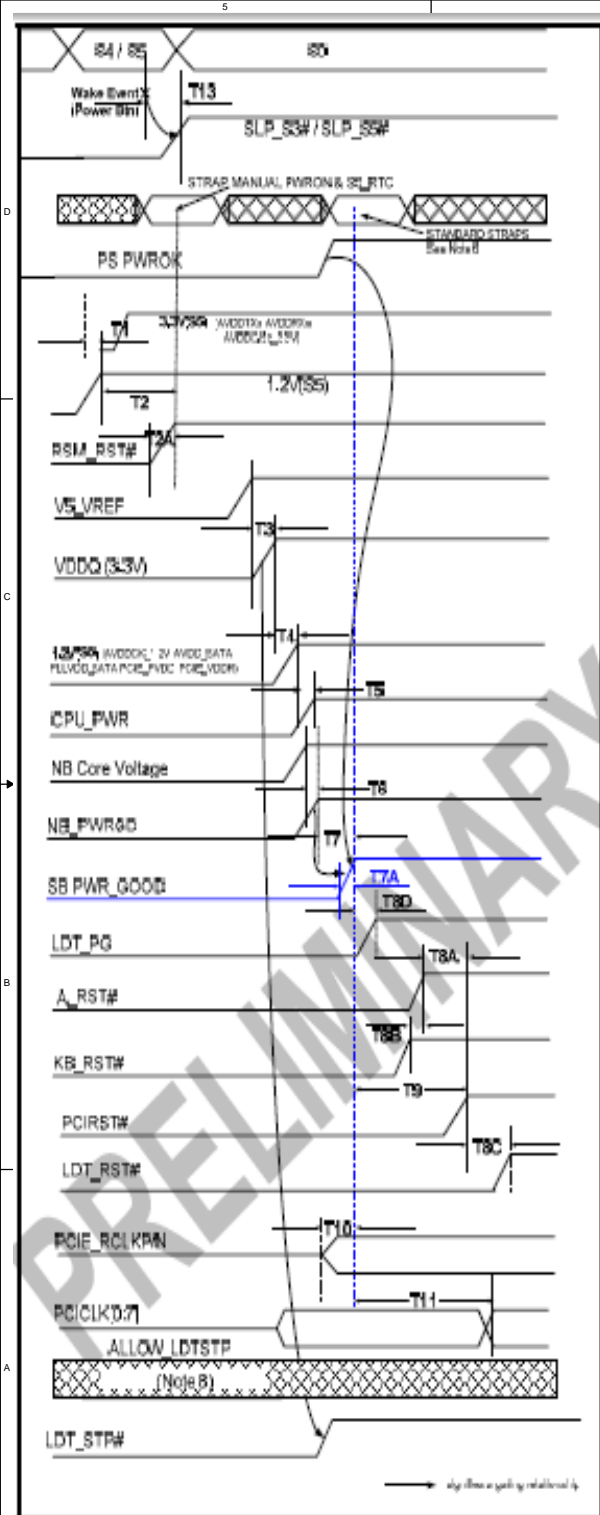
RS780M



U10 & U13 new version (Part number) ?

MICRO-STAR INT'L CO., LTD.			
Title BOM - Option Parts			
Size	Document Number		Rev
	MS-7501		3.1
Date:	Friday, July 25, 2008		Sheet 37 of 40





Micro Star Restricted Secret		
Title	RESET MAP	Rev
Document Number	MS-7501	3.1
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Monday, July 14, 2008
Sheet		39 of 40

1. BOM

Ver.	Description	P/N	OPT	CFG
0A	RS780+SB700+ST6740L+F71882+RTL8111C +ALC888+JMB381+ICS9LPRS477	601-7501-A10		CFG_7501
2.0	RS780+SB700+ST6740L+F71882+RTL8111C +ALC888+JMB381+ICS9LPRS477	601-7501-01S		CFG_7501
2.1	RS780+SB700+ST6740L+F71882+RTL8111C +ALC888+JMB381+ICS9LPRS477	601-7501-04S		CFG_7501
2.1	RS780+SB700+ST6740L+F71882+RTL8111C +ALC888S-VC +VT6308+88SE6111	601-7501-05S	SVC	CFG_7501
3.0	RS780+SB700+ST6740L+F71882+RTL8111C +ALC888S-VC+VT6308+88SE6111	601-7501-10S		CFG_7501
3.0	RS780M +SB700+ST6740L+F71882+RTL8111C +ALC888S-VC+VT6308+88SE6111	601-7501-11S	M	CFG_7501M
3.1	RS780+SB700+ST6740L+F71882+RTL8111C +ALC888S-VC+VT6308+88SE6111			CFG_7501

2.Modify list

7501-2.0

- 1.修改為Medion所要的相關connector規格
- 2.Modify NB heatsink
- 3.Add sata 5 and sata6

7501-2.1

- 1.Modify SATA connector 為90度
- 2.Modify FAN circuit

7501-2.1 OPT:SVC

- 1.Modify Audio為ALC888S-VC
- 2.Remove HDMI and VGA

7501-3.0

- 1.Modify PWM為4+1相

7501-3.0 OPT:M

- 1.Modify NB CHIP TO RS780M

7501-3.1

- 1.Modify PWM LAYOUT

Micro Star Restricted Secret			
Title		Rev	
HISTORY		3.1	
Document Number		MS-7501	
MICRO-STAR INT'L CO.,LTD. No. 68, Li-De St, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Monday, July 14, 2008 Sheet 40 of 40	